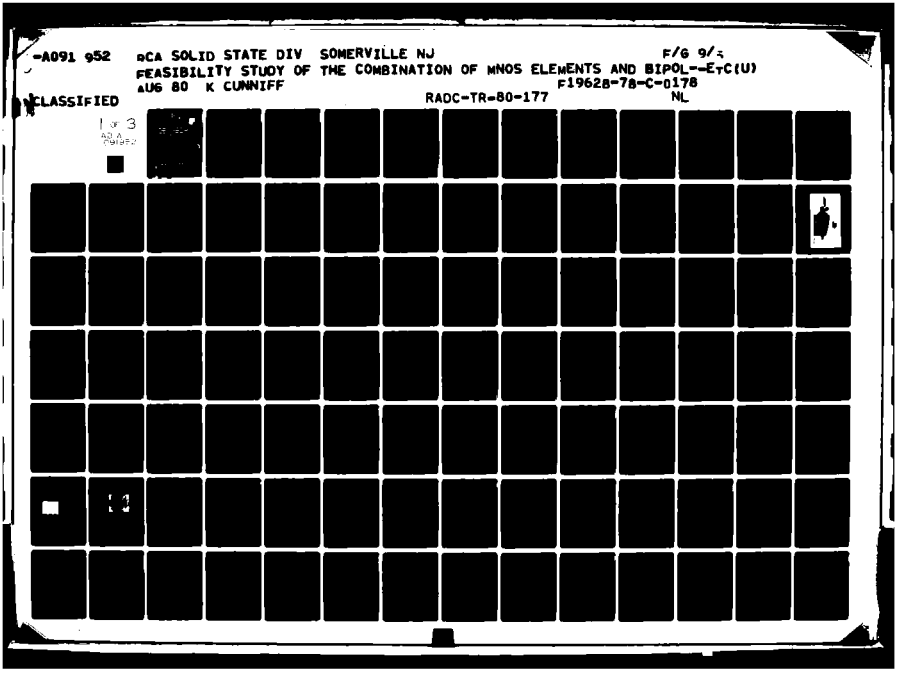

-A091 952 RCA SOLID STATE DIV SOMERVILLE NJ F/G 9/5
FEASIBILITY STUDY OF THE COMBINATION OF MNOS ELEMENTS AND BIPOL--ETC(U)
AUG 80 K CUNNIFF F19628-78-C-0178
CLASSIFIED RADC-TR-80-177 NL
1 OF 3
AD A091952

RADC-TR-80-177
Final Technical Report
August 1980

12
B.S.

FEASIBILITY STUDY OF THE COMBINATION OF MNOS ELEMENTS AND BIPOLAR TTL PERIPHERALS ON AN LSI CIRCUIT CHIP - PHASE I

RCA

Kevin Cunniff

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-80-177 has been reviewed and is approved for publication.

APPROVED: Patrick J. Vail

DR. PATRICK J. VAIL
Project Engineer

APPROVED: Clarence D. Turner

CLARENCE D. TURNER, Acting Director
Solid State Sciences Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

SUBJECT TO EXPORT CONTROL LAWS

This document contains information for manufacturing or using munitions of war. Export of the information contained herein, or release to foreign nationals within the United States, without first obtaining an export license, is a violation of the International Traffic in Arms Regulations. Such violation is subject to a penalty of up to 2 years imprisonment and a fine of $100,000 under 22 U.S.C 2778.

Include this notice with any reproduced portion of this document.

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (ESR) Hanscom AFB MA 01731. This will assist us in maintaining a current mailing list.

Do not return this copy. Retain or destroy.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: RADC-TR-80-177	2. GOVT ACCESSION NO.: AD-A091 952
3. RECIPIENT'S CATALOG NUMBER:	
4. TITLE (and Subtitle): FEASIBILITY STUDY OF THE COMBINATION OF MNOS ELEMENTS AND BIPOLAR TTL PERIPHERALS ON AN LSI CIRCUIT CHIP - PHASE I	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report. 29 Sep 78 - 29 Jun 79
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): Kevin Cunniff	8. CONTRACT OR GRANT NUMBER(s): F19628-78-C-0178
9. PERFORMING ORGANIZATION NAME AND ADDRESS: RCA/Solid State Division, Somerville NJ 08876	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62704H, CDNA0031
11. CONTROLLING OFFICE NAME AND ADDRESS: Deputy for Electronic Technology (RADC/ESR), Hanscom AFB MA 01731	12. REPORT DATE: August 1980
	13. NUMBER OF PAGES: 208
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Dr. Patrick J. Vail (RADC/ESR)

This work was sponsored by the Defense Nuclear Agency under Subtask Code Z990AXTD068 and Work Unit 03.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

MNOS
Memories
Radiation Hardening

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of the reported research was to obtain radiation, reliability, and performance data on monolithic test structures containing MNOS memory transistors and n-p-n bipolar transistors. The data indicates that the devices performed acceptably at 10^5 rads(Si). Thin-oxide structures performed satisfactorily after exposure to 5×10^5 rads(Si). Thus, if these devices were combined into an EAROM memory circuit, a hardness level above 10^5 rads should results. Performance, reliability,

DD FORM 1 JAN 71 1473 EDITION OF 1 NOV 65 IS OBSOLETE (Cont'd)

UNCLASSIFIED

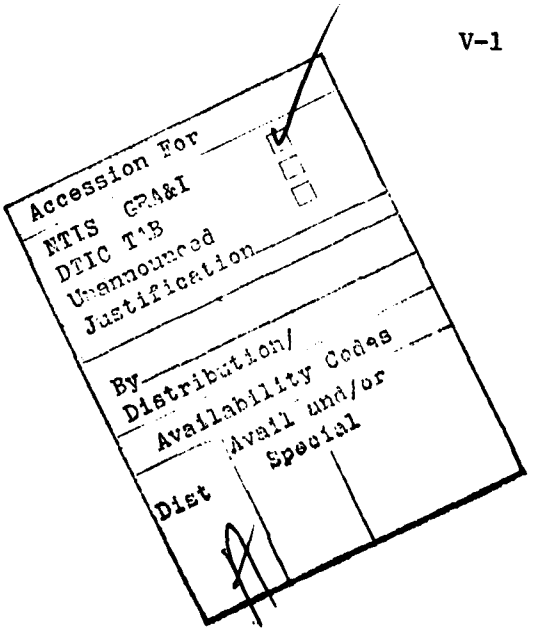
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

405921

Item 20 (Cont'd)

and breakdown characteristics were measured and are consistant with parameter values that would be useful for an EAROM.

TABLE OF CONTENTS



LIST OF FIGURES

LIST OF FIGURES (cont'd)

LIST OF FIGURES (CONT'd)

LIST OF TABLES

EVALUATION

The contractor evaluated a new approach to MNOS memory circuit design that used bipolar circuitry for every function on the memory chip except actual storage of data. The approach has the advantage that it is a commercial process for which there is a large amount of reliability data. The technology looked promising at the start for radiation hardness due to the complete elimination of MOS technology which is notoriously vulnerable to radiation. The results were discouraging, however, because the MNOS transistors proved to be moderately vulnerable to radiation. Although the resulting hardness is one to two orders of magnitude higher than that of most standard commercial MNOS technology, it did not satisfy the goals desired for the specific application which generated the requirement. (Related TPO 4D5)

PATRICK J. VAIL

SECTION I

PREFACE

This report represents the findings and recommendations derived from the feasibility study (Phase I) on the subject in question, conducted under the Contract No. F19628-78-C-0178, administered by Pat Vail, Project Engineer, Rome Air Development Center, Deputy for Electronics Technology.

SECTION II
INTRODUCTION

Previous rad-hard IC's utilizing MNOS transistors as memory elements used MOS control logic (PMOS or CMOS). This study has revealed that the state-of-art MOS circuitry represented the weak link in the rad-hard characteristics. The study also demonstrated that MNOS memory transistors were effective rad-hard memory cells. (Ref: Contract Review on "1K Nonvolatile Memory", held at Westinghouse Co. for the Air Force Material Lab., June 1979).

RCA's Bipolar Design Group developed circuits and process which led eventually to "BIMOS" IC's. There are numerous similarities between bipolar and MOS IC technologies, such as: Starting material resistivities, polarities, processing sequences, and compatibility of isolation and diffusion techniques.

The known radiation performance of bipolar circuitry, coupled with the MNOS memory transistor, offers a high-performance combination.

Three compatible technologies were developed by RCA's SSD (Solid State Division), the integration of which offers an opportunity to generate IC's with conceivably superior radiation tolerances. The technologies of interest are:

1. Dielectric Isolation.
2. Bipolar Processing.
3. MNOS Processing.

RCA's Commercial Design Group is developing several circuits based on combined technologies. One of these circuits utilizes both MNOS and bipolar transistors on the same chip. This circuit was developed for commercial

applications requiring an "EAROM." For the commercial circuits, no radiation tolerance is required.

The p-n junction isolated circuit of interest employs MNOS transistors as memory elements and bipolar transistors for analog and digital circuit functions.

A test key (TA10306) was developed and tailored to facilitate the evaluation of special parameters and functions of the devices representing the hybrid technology. This test key was used as a test vehicle in all the studies reported in subsequent sections of this report. The test key pellets employed in this study were derived from wafers processed in the IC engineering model shop by the standard commercial process without any regard whatever to the rad-hard capability of the resulting devices.

The test key incorporates all the elements of the technologies which are presently used in the High Speed Bipolar IC operation and are utilized in production of rad-hard IC's except dielectric isolation.

The merger of the above processes makes possible a dielectric isolation MNOS/Bipolar, rad-hard process suitable for re-entry "EAROM" applications.

SECTION III
STATEMENT OF WORK

A. OBJECTIVES OF PHASE I

1. Credits:

The R&D study, the subject of this report, was sponsored and funded by the Electronics Systems Division (PKR), Air Force Systems Command, U.S. Air Force, Hanscom Air Force Base, MA 01731.

The primary objectives of the reported research were to fabricate n-p-n bipolar transistors and MNOS devices on the same chip, to assess the gamma radiation performance of these structures, and to determine whether these devices could be combined into a radiation-tolerant memory design. The data derived from the feasibility study is to be used for guidance in selecting the radiation-hardened 1K "EAROM" design.

The TA10306 circuit was chosen for Phase I analysis since it is immediately available and represents the processing technology which can be utilized for Phase II effort. This circuit provided a fringe benefit in the sense that any influences exerted by the bipolar processing could be detected and verified by this test key.

In the testing and characterization of the devices of interest, the primary emphasis was placed upon the following parameters:

- V_{TH} - initial threshold.
- Fixed amplitude switching at 25V and 30V.
- Gm - transconductance.
- Retention time through a latitude of duration.
- Erase/write degradation.
- Total-dose radiation.
- Bipolar transistor characteristics, such as: Gain, V_{BD}, V_{CE}(sat), leakage current.

The devices were irradiated to predetermined gamma dose levels by means of the Gammacell-220 radioactive GBAL irradiator; the above-listed parameters were used as the yardstick to ascertain the rad-hard characteristics of the test vehicle (TA10306).

B. TECHNICAL APPROACH

The program was divided into the following sequence of tasks:

1. Fabrication of test chips.
2. Zero-hour characterization of the test chips.
3. Irradiation (Gamma - total dose of the chips).
4. Post-radiation characterization.
5. Reliability testing and failure analysis.
6. Summary - conclusions - recommendations.

The Engineering Model Shop facilities of the High-Speed Bipolar IC operation were utilized to generate the device wafers required for this study. No major problems were anticipated in merging the dielectrically isolated bipolar devices with MNOS processing. Basically, these processes are technologically compatible. However, most TTL circuits require a maximum voltage of 7 volts, which is determined by BV_{CEO} The MNOS devices require up to 30 volts for programming. Consequently, minor adjustments to the TTL process were made to accommodate the higher MNOS voltage requirements. An appropriate set of masks (TA10306) was made for p-n junction processing.

The TA10306 chip incorporated both drain-source protected and thin-oxide transistors. The drain-source protected unit is the one of major interest, but the thin-oxide unit was required as a reference so that the effects of the thin-oxide region and the thick-oxide region of a drain-source protected device could be carefully separated.

A "stepped oxide" MNOS transistor channel is actually a composite device consisting of a thin-oxide (20Å) memory portion centered between thicker oxide (500Å) fixed threshold sections. This transistor exhibits enhancement-mode operation with source-to-drain breakdown voltage in excess of 35 volts,

and is best suited for use in the design of large-scale nonvolatile memories.

The testing procedures make use of the saturated threshold voltage state as a reference level on which all tests can be based.

The thin device is used in conjunction with the stepped-oxide MNOS transistor for evaluating the saturation into the high-conduction state because the high-conduction state typically exhibits depletion-mode behavior for the thin-oxide memory portion of the transistor. In the stepped-oxide MNOS device, the depletion-mode characteristics of the thin-oxide characteristic of the thin-oxide portion of the device is suppressed by the characteristics of the thick-oxide portion.

The thicker oxide region results in a fixed-threshold nonprogrammable enhancement-mode transistor. The stepped-oxide device will be dominated by the thick-oxide section when the thin-oxide threshold voltage is more positive than that of the thick-oxide portion. By having both devices, these characteristics can be separated.

In order to provide a broad statistical basis, the devices used in this study were derived from four different wafer process lots which were processed in an identical manner. Table III-1 summarizes the technological highlights of the process employed. Table III-2 represents a detailed process flow-sheet, and incorporates the more important process and quality-control points. Fig. III-1 shows the vertical geometry of devices formed by the above described process.

Characterization of the four lots has revealed that three lots provided normal, expected characteristics, but that the fourth lot exhibited poor retention characteristics. An analysis of the defective lot revealed that the quality of the silicon nitride was poor. This kind of wafer would normally be eliminated by the initial wafer acceptance test; consequently, this lot was replaced with another meeting the specifications.

Table III-1 - Processing Steps

Pocket (S_B)

*ISO

*Deep N+

Arsenic Field Implant

I^2L Base

B & R

Emitter N+

Channel For MOS

Channel For MNOS

*(First Contact (Thermal Nitride)
(Second Contact (Underlying Oxide)

Metal

Protect

13 Mask Levels Plus 3 Redundant Levels

*Redundant Masking Level

Table III-2 - Process and Quality Controls

1.	Starting substrate wafer (1-0-0), P- doped 25 - 50 Ω cm	Q.C.
2.	Preoxidize and oxide strip cleaning	
3.	Oxidize at 1000°C steam ~ 2 hours	T_{ox}
4.	N+ photoresist and oxide etch	Visual
5.	Antimony deposit 1250°C	
6.	Glass removal steam oxidation at 1200°C	R_s
7.	Strip oxide	Visual
8.	Grow Epi layer (N- doping) 1.6 - 1.5 Ω cm typical 8μm thick	Layer thick Layer R_s Visual
9.	Steam oxidation 1000°C - 2 hours	T_{ox} Visual

Table III-2 - Process and Quality Controls (cont'd)

10.	ISO photoresist and oxide etch	Visual
11.	ISO Boron deposit (B.S.G. C.V.D.) and anneal 1150°C, N_2	R_s
12.	Boron glass removal diffuse 1200°C O_2/N_2 Strip oxide	Visual
13.	ISO probe	60V
14.	1000°C steam oxidation	T_{ox}
15.	Photoresist both sides develop front N+ collector oxide etch	Visual
16.	N+ deposition ($POCL_3$) 1050°C	R_s
17.	1000°C steam oxidation	T_{ox}
18.	P+ photoresist and oxide etch boron deposit (B.S.G. C.V.D.)	Visual

Table III-2 - Process and Quality Controls (cont'd)

19.	P+ anneal 1100°C N_2/O_2 R_s 5.5 - 6.5 Ω/□ .	R_s
20.	10% HF etch P+ drive-in 1165°C steam	
21.	Field implant photoresist and oxide etch	Visual
22.	Implant arsenic 150 KEV 3 X 10^{12}	
23.	Strip oxide, clean steam, 1165°C R_s 2000 - 2500 Ω/□	R_s
24.	I^2L B&R deposition B.S.G. (C.V.D.) Anneal 945°C R_s 60 - 65 Ω/□	R_s
25.	Remove glass I^2L drive-in steam - 1000°C R_s 230 - 300 Ω/□	R_s
26.	Standard B&R photoresist and oxide etch B.S.G. deposit and anneal at 945°C R_s = 50 - 55 Ω/□	Visual R_s

Table III-2 - Process and Quality Controls (cont'd)

27.	Remove glass diffuse at 1100°C wet/dry R_s I^2L = 325 - 375 Ω/□ R_s B&R = 180 - 230 Ω/□	R_s
28.	Emitter photoresist and oxide etch	Visual
29.	$POCL_3$ deposition 1050°C	R_s
30.	Final oxidation Azeotropic HCL at 940°C	T_{ox}
31.	Channel oxide photoresist and oxide etch "50:1" etch, clean	Visual
32.	Channel oxide oxidation Azeotropic HCL 800°C T_{ox} 600 - 650 Å	T_{ox}
33.	Thin channel photoresist and oxide etch retain photoresist	Visual
34.	Implant phosphorous 35 KEV 5 X 10^{12}, base P.R., B.E. 7 Min. strip photoresist	Visual T_{ox} (channel) 450 - 500Å

Table III-2 - Process and Quality Controls (cont'd)

35.	Thin oxide oxidation Azeotropic HCL, 580°C 35 Min. T_{ox} 18 - 22Å	T_{ox}
36.	Deposit Si_3N_4 (L.P.C.V.P.) 500 - 550 Å	T_{sn}
37.	CV plot for CMOS	ΔV
38.	Anneal at 1000°C in F.G.	
39.	Deposit undoped SiO_2 (C.V.D.) N 5000Å first contact photoresist oxide etch, SiN etch	T_{ox} Visual
40.	Final oxidation Azeotropic HCL 94°C Anneal F.G. 15 Min.	
41.	Anneal F.G. 740°C - 16 hours	
42.	Second contact photoresist and oxide etch clean	Visual

Table III-2 - Process and Quality Controls (cont'd)

43.	Evaporate aluminum metal photoresist and etch	T_{met} Visual
44.	Alloy aluminum 530°C F.G.	
45.	Silane protect (C.V.D.-P.S.G.) 7500 - 9000Å	T_{ox}
46.	Protect photoresist and oxide etch	Visual
47.	W.E.T. backlap circuit probe	
48.	Sell to Assembly Department	

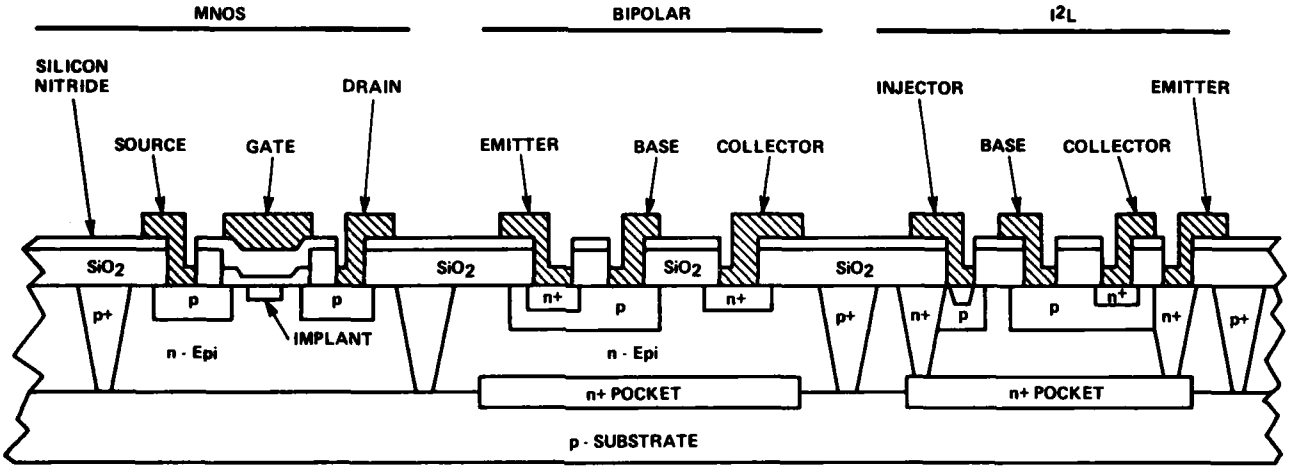


Fig. III-1 - MNOS/I^2L cross-sectional view.

C. RAD-HARD EVALUATION OF THE DEVICES - GENERAL

The IC's used in this study were tested at various (total) doses of "gamma" radiation. The testing was carried out through the use of a Gamma-cell-220, cobalt-60 irradiator available in the Somerville SSD Engineering Labs, Fig. III-2.

The devices to be tested were inserted into a test panel, Fig. III-3, where the MNOS circuits were biased at -10 volts during the irradiation. Specified exposure times were employed to attain the desired total dose. All of the devices were tested immediately before irradiation ("zero hour") and immediately after irradiation for the following electrical parameters:

1. Bipolar Beta at = 10 μA
   100 μA
   1 mA

   V_{CEO}
   V_{CBO}
   V_{EBO}
   $V_{CE}(sat)$
   I_{CEO}

2. MNOS: V_{TH} Volts

Subsequently, the devices were returned to the RCA David Sarnoff Research Labs in Princeton for other tests stipulated by the contract.

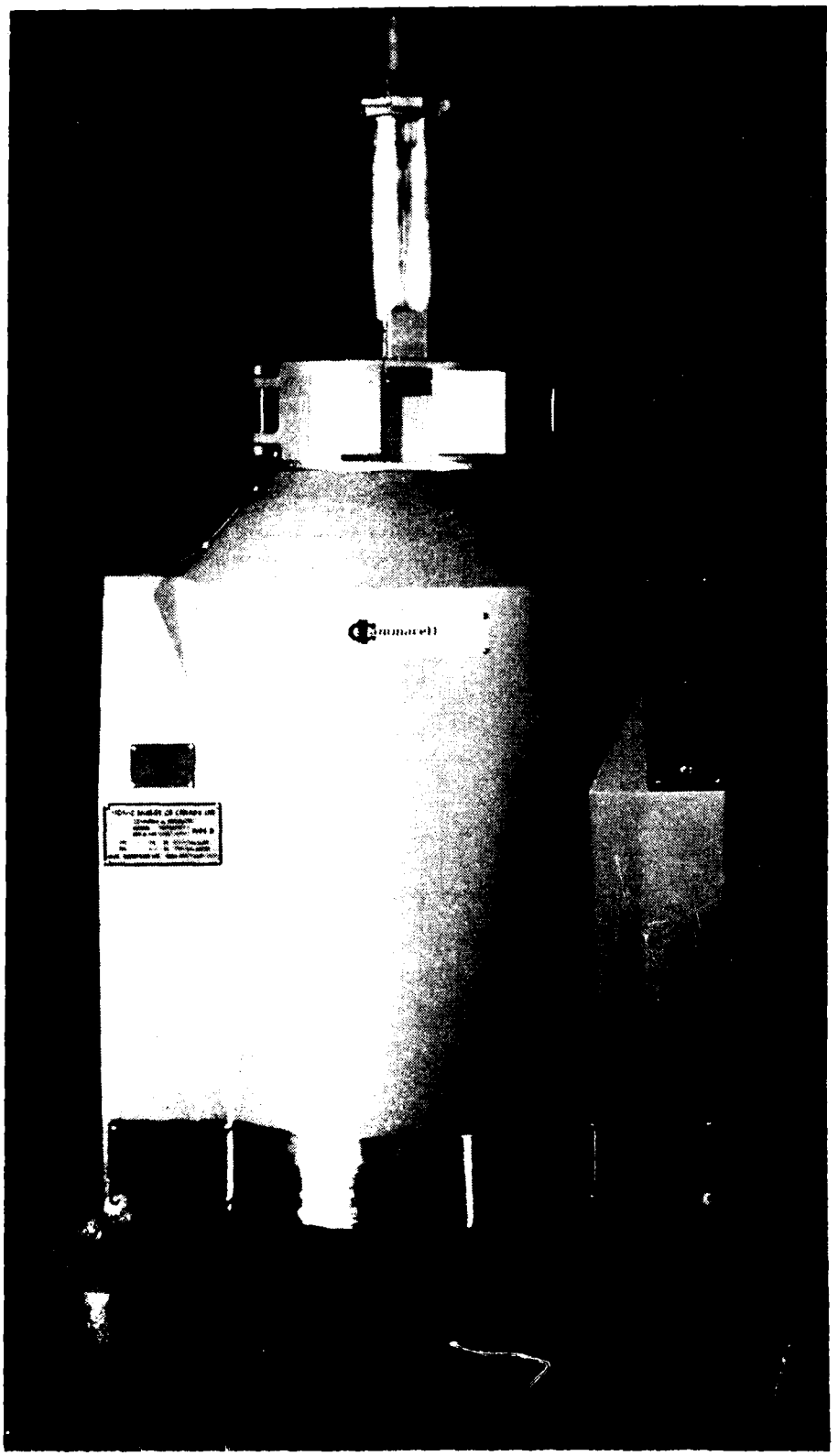
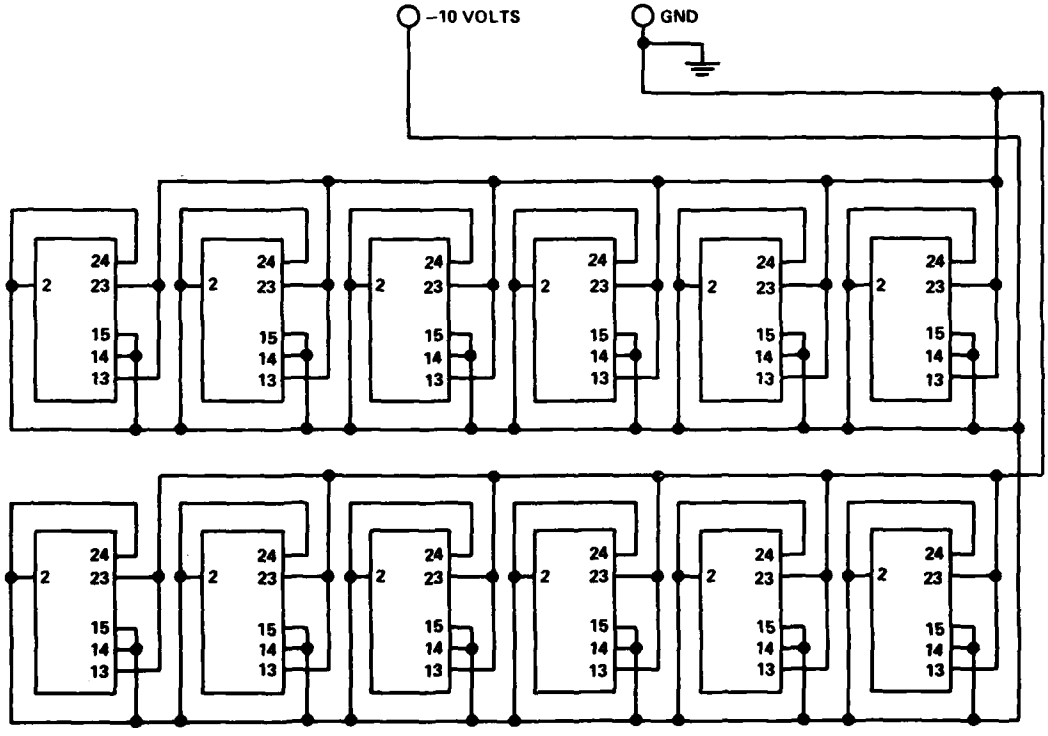


Fig. III-2 - Gammacell 220.



Note: For pinouts see pages A-21 and A-33.

Fig. III-3 - TA10306A radiation test board.

SECTION IV
ELECTRICAL TESTING OF DEVICES *

A. INTRODUCTION

The testing of the MNOS devices fabricated with bipolar transistors was aimed at finding those characteristics pertinent to nonvolatile memory design that existed for representative devices in the TA10306 test array. The testing involved twenty packaged devices from four different diffusion lots. The test flow chart is shown in Fig. IV-1 (See Appendix).

B. TEST EQUIPMENT

A block diagram of the basic test equipment used to evaluate the MNOS devices is shown in Fig. IV-2. The device under test (D.U.T.) is accessed through a relay matrix by a V_{TH} sample measurement system and a programmable pulse generator. The control-logic section adds automatic preselected control of pulse and V_{TH} read operations. A more detailed functional block diagram is given in Fig. IV-3. It is clear that the operator can choose pulse amplitude and duration for driving the MNOS element and the time selection (in decades) of V_{TH} read for retention-time measurements. The measured data is digitized and transferred onto magnetic tape by a SERDEX data acquisition system. The data was transferred from the cassette type to disk file on a Data General Eclipse C300 computer to allow automatic plotting of the data.

In the case of retention data, an option in the plotting package was selected to fit a least squares line through the data points. The values of the fitting parameters are automatically notated on the left edge of each plot. The values shown correspond to the fitting parameters for the line $Y = m x + b$, where X = log (time) and Y = threshold voltage. Given in this form, the value of m noted on the graph corresponds to the change in threshold voltage per decade of time. For the stepped-oxide devices, there was generally no change in threshold when the device was first written to the low threshold state, so that the slope shown is zero. (An error in the calculation routine shows this data with a correlation coefficient, R, of zero rather than 1.000. The correlation coefficient for all other cases is calculated correctly.)

---

* All Figures and Tables for Section IV are contained in the Appendix.

Fig. IV-4 through 12 contain more detailed block diagrams of each major subsection of the test system. Fig. IV-13 through 21 detail the actual circuitry used in each of the major blocked sections of the system.

In order to assure highly accurate and reproducible measured results, the calibration procedure shown below was adopted:

1. Only the resistors which had been designated for this procedure were used since these were the only ones whose actual values were known.
2. The resistor to be used was connected directly to the current-source output on the back of the threshold-measurement system.
3. A pulse generator was connected to the ext. clock input and the rep. rate varied until the digits on the DVM changed at approximately a 10 Hz rate.
4. The top cover was removed, and the pot which corresponded to the current range selected was adjusted.
5. When the adjustment was deemed correct, the INT./EXT. switch was flipped to internal, and at least 9 or 10 readings of the same voltage were taken. The average was taken to be the expected reading, it should be within 390.
6. If averaged readings were not within 390, steps 4 and 5 were repeated.

The resistors used for calibration are shown in Table IV-1; the actual values of the specific calibration resistors used are shown in Table IV-2. The tables show that precision resistors are used to calibrate the various current ranges. The measured linearity of the V_{TH} measurement system for each current scale is shown in Figs. IV-22 through IV-29.

Since the V_{TH} measurement is a sample read of the turn-on voltage of the MNOS FET, a critical parameter associated with it is the time duration of the gate-to-source voltage during reading. The tradeoff decided was to minimize the sample-read duration, but not to cut off the read at the 1 microampere current range for a device with a large negative V_{TH}(approximately -18V). The value selected was 6 milliseconds. V_{TH} timing information is shown in Fig. IV-30.

C. TA10306

The TA10306 test key was selected as the vehicle for evaluation of the MNOS FET devices. This test key consists of a stepped-oxide (drain-source protected) MNOS and a thin-oxide only MNOS device bonded out separately in a 24-pin ceramic, hermetically sealed, dual-in-line package (DIC). This test key also has a bipolar n-p-n device bonded out. A photomicrograph and bond-out diagram is shown in Fig. IV-31.

D. TEST RESULTS

The first part of the test flow shown in Fig. IV-1 required the documentation of the initial V_{TH} of both the stepped-oxide and thin-oxide MNOS devices. These devices are tested as received from fabrication and packaging and have received no programming pulses. The measured values are shown in Table IV-3.

The V_{BD} or the source-to-drain breakdown voltage was measured for all units selected for further testing, as shown in the flow of Fig. IV-1. The measurement was made with the gate and source fixed at ground and with a forced drain potential. The voltage needed for an I_{DS} of 1 microampere was measured; the results are shown in Table IV-4.

The testing is divided into measurements of retention time and fixed-amplitude-switching (FAS) characteristics. The units are further subdivided into 25-volts and 30-volts pulsed devices. Typical graphs for fixed-amplitude switching and retention time are included in Figs. IV-32 and IV-33.

The fixed amplitude switching measurement, Fig. IV-32, plots the threshold voltage of the device after it has been pulsed with a 25 or 30-volt pulse whose width is varied from the microsecond range up to a tenth of a second. The threshold voltage is changed from the high-conduction state that is +1 volt to the low conduction state, -6 volts, with each set of measurements. Examination of the typical graph in Fig. IV-32 shows that the threshold voltage reaches a low limit after a pulse of 25 volts with a 10 millisecond width.

The retention-time graph in Fig. IV-33 plots the threshold voltage versus time for an MNOS device. The device is pulsed into the low conduction state with a 25-volt pulse with a width of 10 milliseconds. The threshold voltage is measured after the indicated elapsed time; i.e., from a minimum of 0.01 seconds to a maximum of 10,000 seconds. The slope of the line obtained gives an indication of the long-term stability of the structure.

The results of the tests are presented by lot. As shown in Table IV-4, the four diffusion lots were taken from lots No. 2A, 10A, 13A, and 18. The slope of the least-squares line through the data, m, gives the rate of change of threshold in volts/decade of time.

1. Lot 2A

a. 25V. Figs IV-32 through IV-37 display the FAS at 25°C of units No. 3, 8, and 9 for both the thin-oxide (TO) and stepped-oxide (SD) devices. Figs. IV-38 through IV-40 display the FAS for unit No. 1 for -55°C, 25°C, and 125°C. Figs IV-41 through IV-44 show the retention time at 25°C for thin and stepped-oxide (TO and SO) devices.

b. 30V. Figs IV-45 through IV-50 display the TO and SO characteristics at 25°C. Fixed-amplitude switching characteristics, FAS, for unit No. 5 at 25°C and 125°C are shown in Figs. IV-51 and IV-52. Retention times for TO and SO devices at 25°C are shown in Figs. IV-53 through IV-58.

2. Lot 10A

a. 25V. Figs. IV-59 through IV-64 display FAS for TO and SO at 25°C. Retention time is shown at 25°C in Figs. IV-56 through IV-70 for SO and TO.

b. 30V. Figs. IV-71 through IV-76 display FAS for TO and SO at 25°C. Retention time is shown in Figs. IV-77 through IV-82 for SO and TO at 25°C.

3. Lot 13A

a. 25V. Figs. IV-83 through IV-88 display the FAS for TO and SO at 25°C. Retention time is shown in Figs. IV-89 through IV-94 at 25°C.

b. 30V. Figs. IV-95 through IV-100 display FAS for TO and SO at 25°C. Retention time is shown in Figs. IV-101 through IV-106 at 25°C.

4. Lot 18

a. 25V. Figs. IV-107 through IV-112 display the FAS for TO and SO at 25°C. Retention time is shown in Figs. IV-113 through IV-118 for TO and SO at 25°C.

b. 30V. Figs. IV-119 through IV-124 display the FAS for TO and SO at 25°C. Retention time is shown in Figs. IV-125 through IV-130 for TO and SO at 25°C.

The FAS for TO devices at 25°C are shown in Figs. IV-131 through IV-137 for lot 2A, in Figs. IV-138 through IV-140 for lot 10A, in Figs. IV-141 through IV-146 for lot 13A, and Figs. IV-147 through IV-151 for lot 18.

E. BIPOLAR TRANSISTOR RADIATION DATA

The n-p-n transistors which were processed on the same test key as the MNOS devices were subjected to gamma radiation. Data is presented in Table IV-5 on the test done at 1×10^5 and 5×10^5 rads. The degradation which is evident at 5×10^5 rads is typical of devices which are processed without concern for radiation tolerance.

The data shows degradation of beta at a collector current of 10 micro-amperes. The beta is reduced by a factor of 2.5 to 3 times its initial value as a result of the generation of surface states at the emitter base junction boundary. Improvements in this performance can be obtained by modifying the oxidation and annealing conditions after the emitter diffusion step. n-p-n transistors which perform satisfactorily after exposure to 1×10^6 rads are fabricated in the High-Speed Integrated-Circuit production area. These devices are being utilized in a number of military systems.

F. MNOS RADIATION TEST RESULTS

Tables IV-6, 7, and 8 show the radiation test results of the thin-oxide and stepped-oxide devices after exposure to the 1×10^5, 5×10^5 and 1×10^6 rads. Analysis of the Table IV-6 shows that a window of voltage exists for both the thin and stepped-oxide device after exposure to 1×10^5 rads.

Table IV-7 shows that the performance of the thin-oxide devices is acceptable after exposure to 5×10^5 rads.; i.e., the voltage window between the high-conduction state and the low-conduction state is at least 1 volt. The stepped-oxide device has degraded so that only three of the nine units have an acceptable window between the high and low states. The thicker oxide in the stepped-oxide device has caused the degradation. Devices made with thin oxide perform satisfactorily at this level.

At 1×10^6, Table IV-8, both the thin-oxide and stepped-oxide devices have degraded to an unusable level.

The oxidation procedure which was used to fabricate the 1000-A thick oxide can be modified so that it will have acceptable characteristics at 1×10^6 rads. RCA has fabricated MOS devices which demonstrate this capability. This test has demonstrated that the thin-oxide nitride structure must be improved if it is to survive the 1×10^6 rads exposure. It should be noted that the thin-oxide structure is not acceptable by itself as a memory element.

The stepped-oxide device was designed to overcome two deficiencies of the thin-oxide structure. The thin-oxide structure can become a depletion mode MOS device. With a thick-oxide device connected in series, the composite structure stays in the enhancement mode. The stepped-oxide region covers the source-to-substrate and drain-to-substrate junctions. Thin-oxide structures exposed to high-temperature bias life tests exhibited a high incidence of failures for leakage current. Use of the stepped-oxide structure eliminated this problem.

G. LIFE AND WRITE/ERASE DATA

Data is presented in Figs. IV-152 through IV-155 on parts fabricated in the Model Shop.

Fig. IV-152 presents 25° storage data on 25 units showing average σ and 3 σ limits. The data shows that a window of at least 3 volts exists after 229 days. Projected performance shows a window of 2.5 volts at 9.6 years.

Fig. IV-153 presents data on four units stored at 150°C for 1 year. The data shows a voltage window of 1.8 volts after 1 year storage.

Figs. IV-154 gives data on 27 units which were programed through the write-erase cycle 10^3 times. The devices were then stored at 100°C for 27 hours. Failed units appear to be typical short-term burn-in failures.

Figs. IV-155 gives data on units that were programed through 10^5 write/erase cycles and exposed to 100°C storage. Data was taken at 2.7 hours and 27 hours.

The results of the data described above indicate that the MNOS process is capable of producing devices which will perform satisfactorily over extended periods of time.

SECTION V
CONCLUSIONS

The primary objectives of the reported research were to fabricate n-p-n bipolar transistors and MNOS devices on the same chip, to assess the gamma radiation performance of these structures, and to determine whether these devices could be combined into a radiation-tolerant memory design.

1. The radiation data indicates that the devices performed acceptably at 1×10^5 rads. The thin-oxide structures were acceptable after exposure to 5×10^5 rads.

Analysis and process refinements would be required on the basic thin-oxide nitride structure to make it acceptable at 1×10^6 rads.

2. The electrical performance of the n-p-n transistors was acceptable. Improvements in the oxidation procedures would improve the post-rad low-current performance.

3. The breakdown voltage of the MNOS device exceeds 30 volts. This capability permits the implementation of a write/erase function in the memory of an LSI designed for 30-volt operation.

Therefore, this research has demonstrated that the circuit elements described could be combined into a memory design which would perform acceptably at 1×10^5 rads.

There is no question that a substantial improvement of the rad-hard characteristics can be achieved by observing more processing sophistication in the oxidation procedures. A specific reference is made here to the Rad Hard CMOS Channel Oxide process developed and refined by the RCA Solid State Division under the sponsorship of Wright Patterson A.F.B., Material Lab.

(Contract #F-33615-76-6-5374, W.P.A.F.B., Manufacturing Technology Division, Materials Lab.). The channel oxide process described in this report should be compatible both in sequence and thermally with the MNOS technology employed and described in the present report.

Appendix A

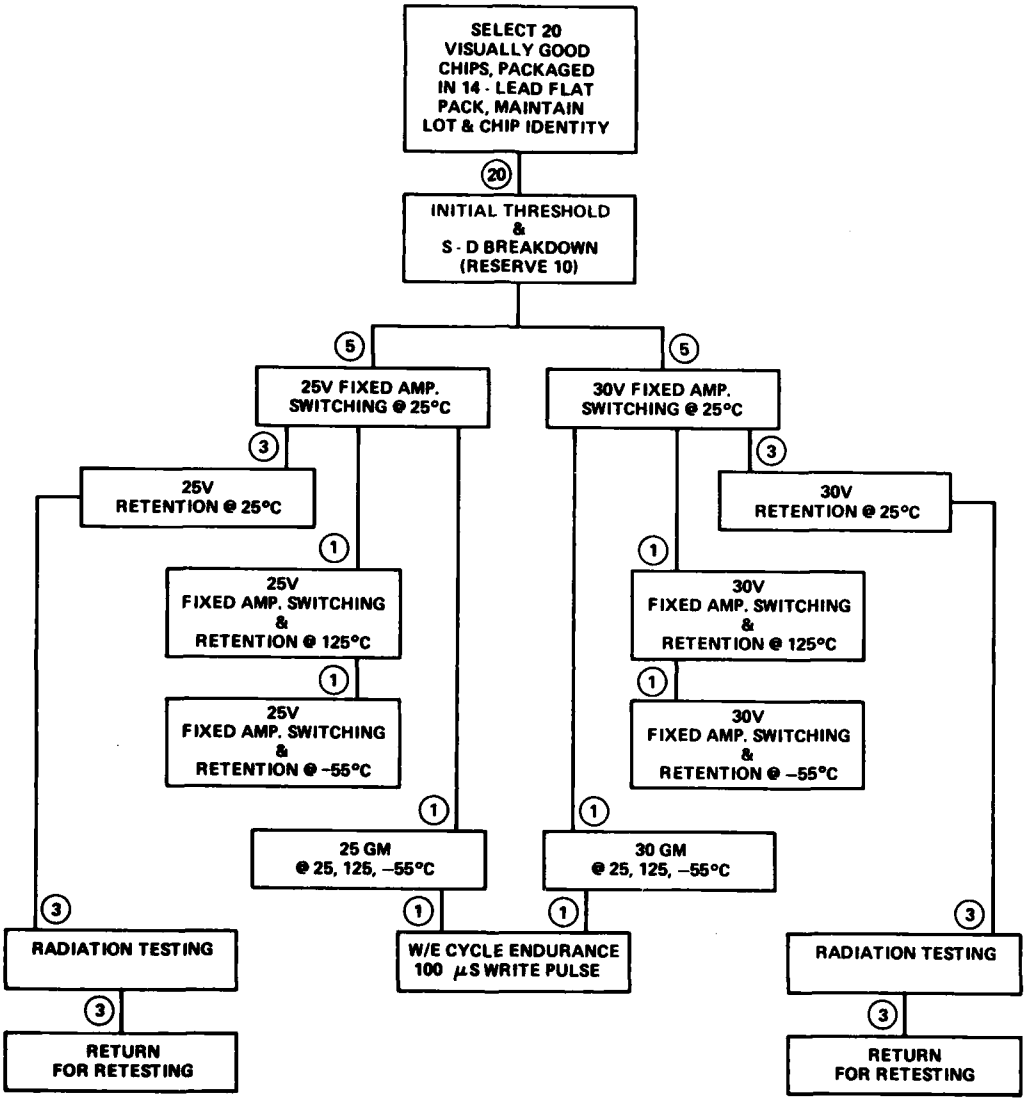


Fig. IV-1 - Radiation-hardened MNOS testing plan (repeated for a total of four lots).

BLOCK DIAGRAM OF DATA AQUISITION SYSTEM

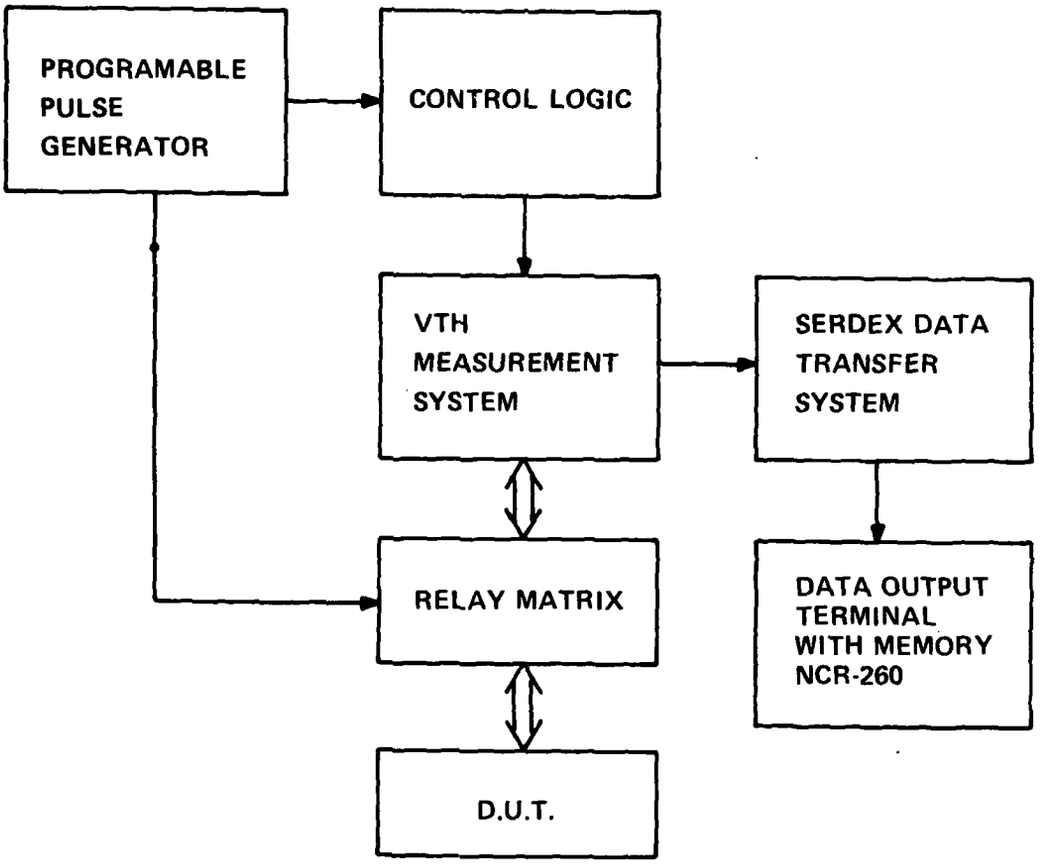


Fig. IV-2 - Block diagram of data acquisition system.

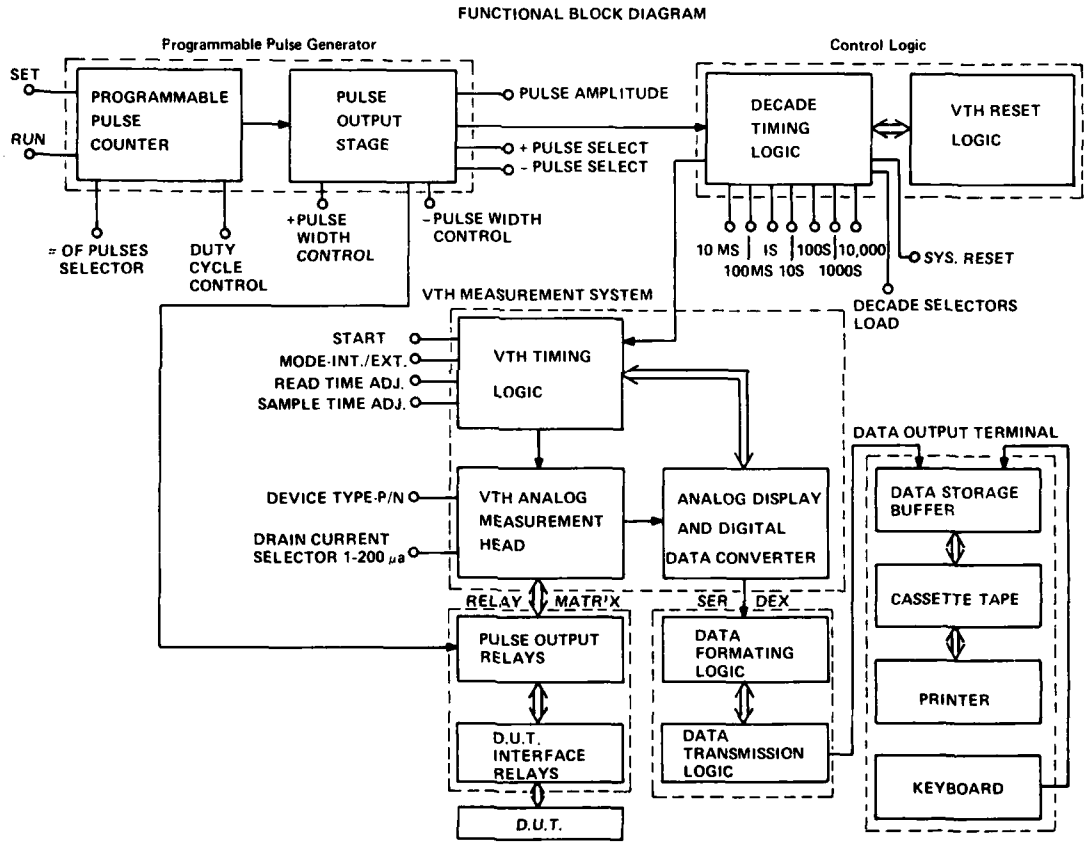


Fig. IV-3 - Functional block diagram.

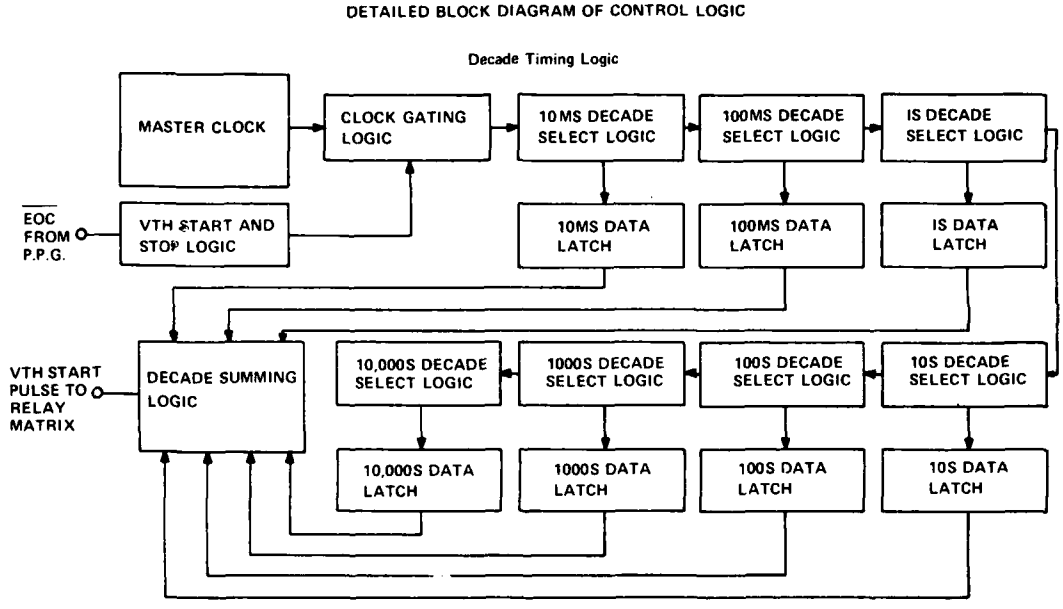


Fig. IV-4 - Detailed block diagram of control logic.

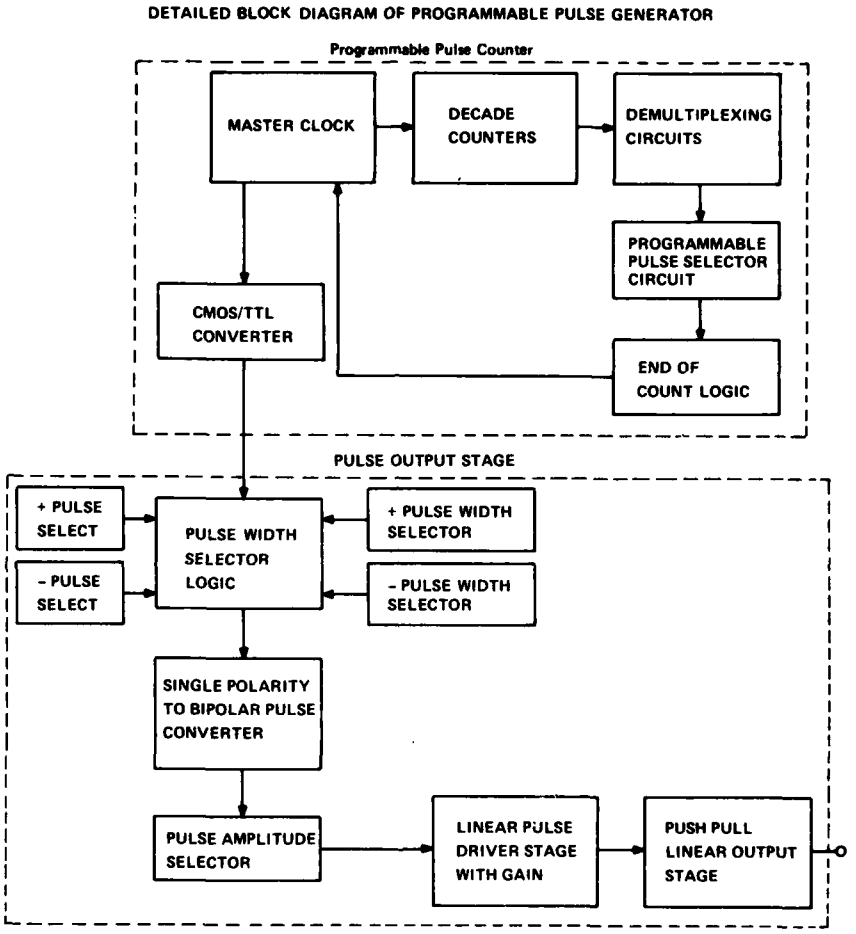


Fig. IV-5 - Detailed block diagram of programmable pulse generator.

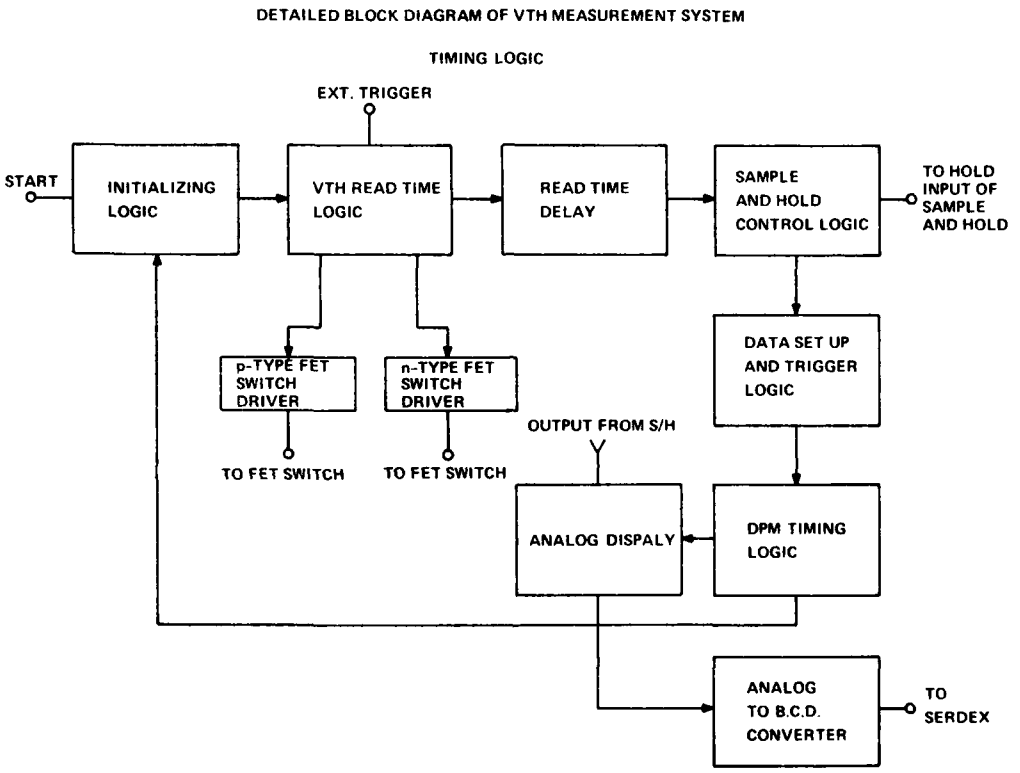


Fig. IV-6 - Detailed block diagram of V_{TH} measurement system.

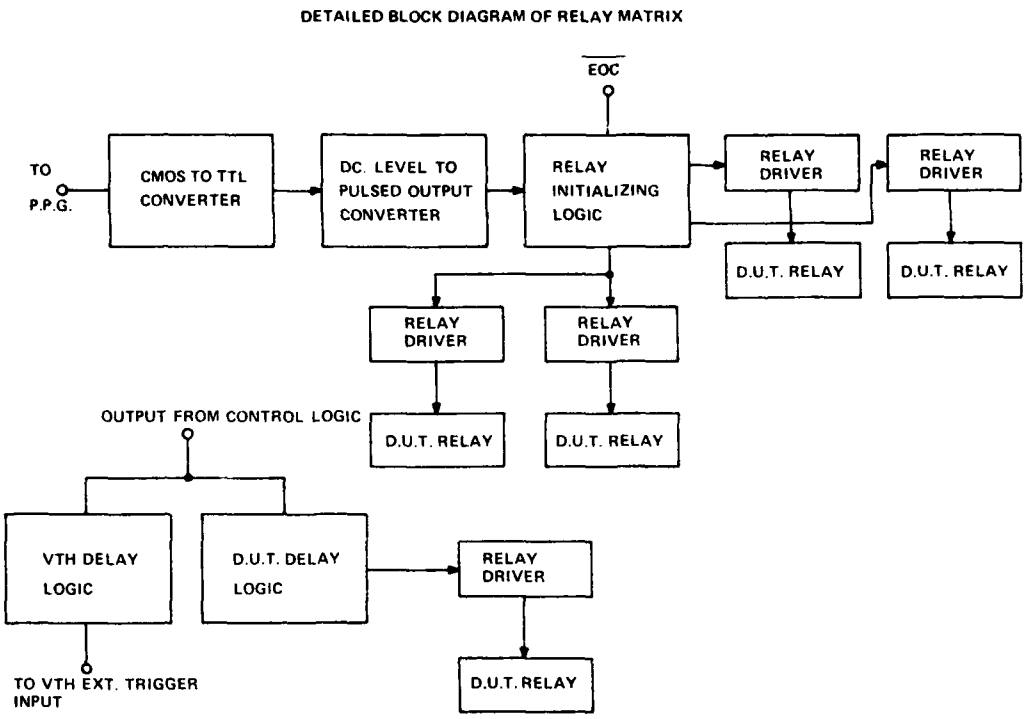


Fig. IV-7 - Detailed block diagram of relay matrix.

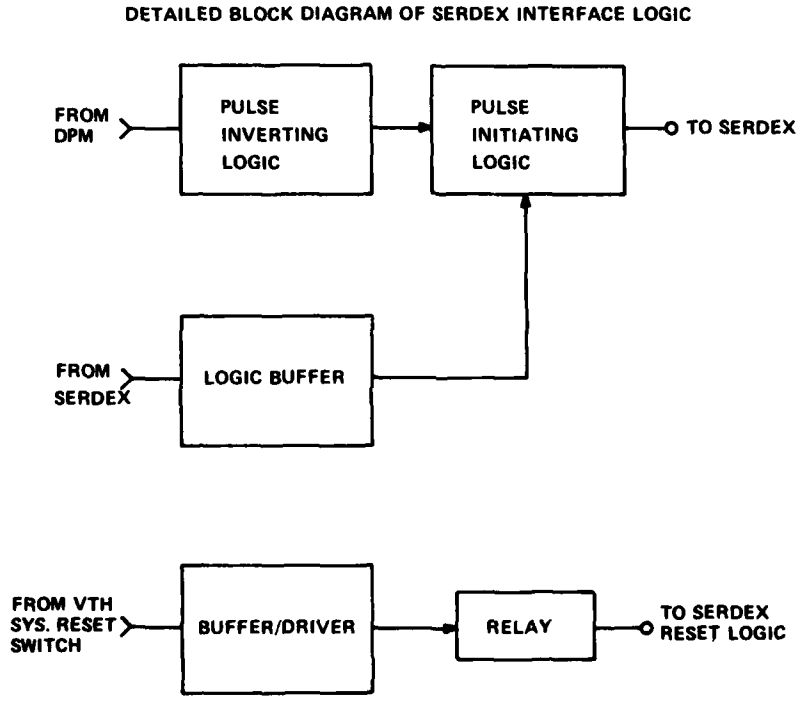


Fig. IV-8 - Detailed block diagram of SERDEX interface logic.

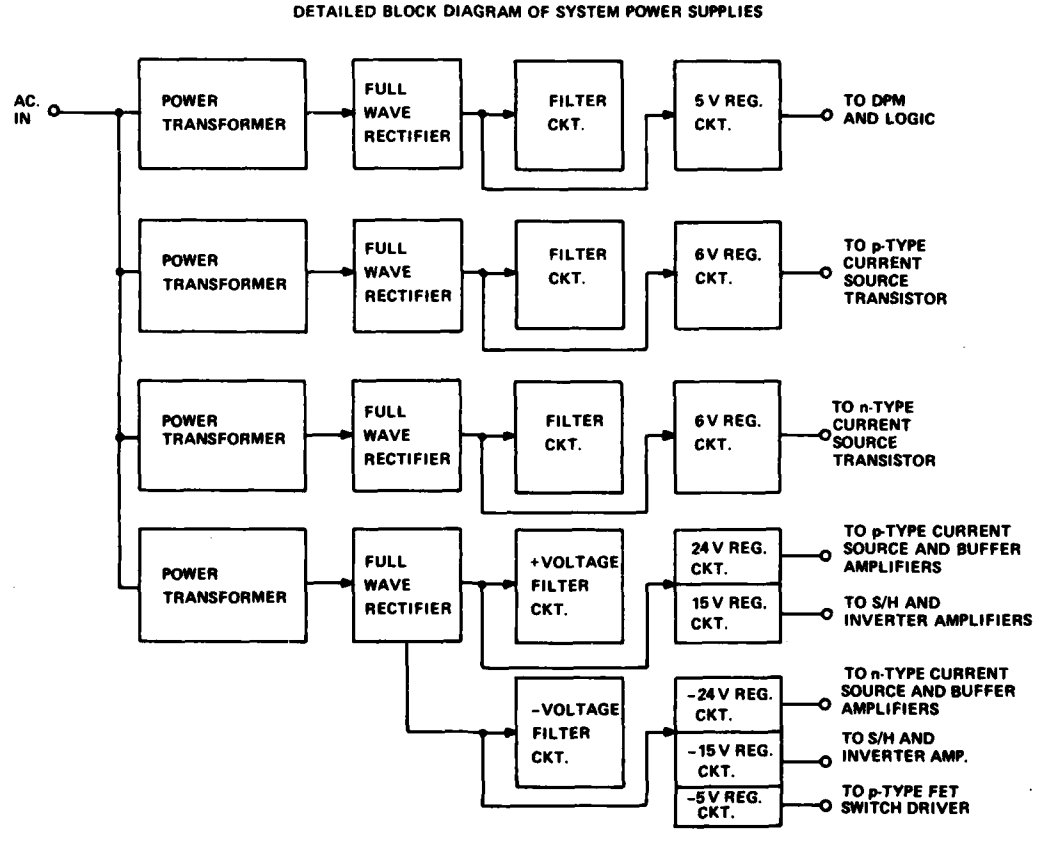


Fig. IV-9 Detailed block daigram of system power supplies.

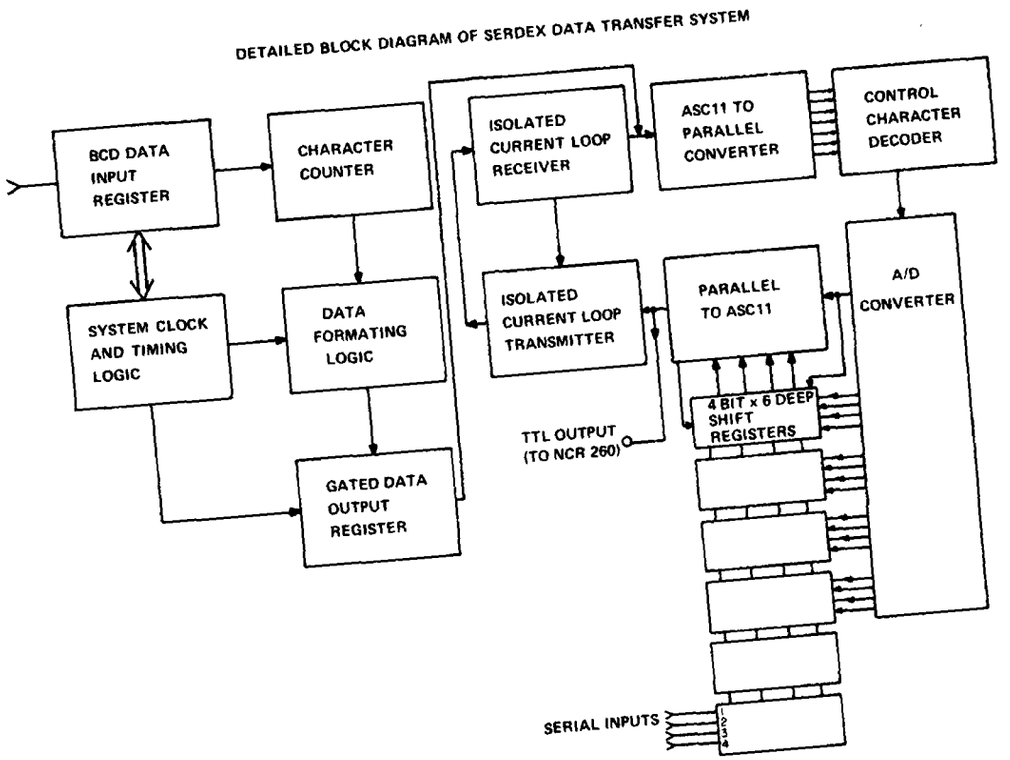


Fig. IV-10 - Detailed block diagram of SERDEX data transfer system.

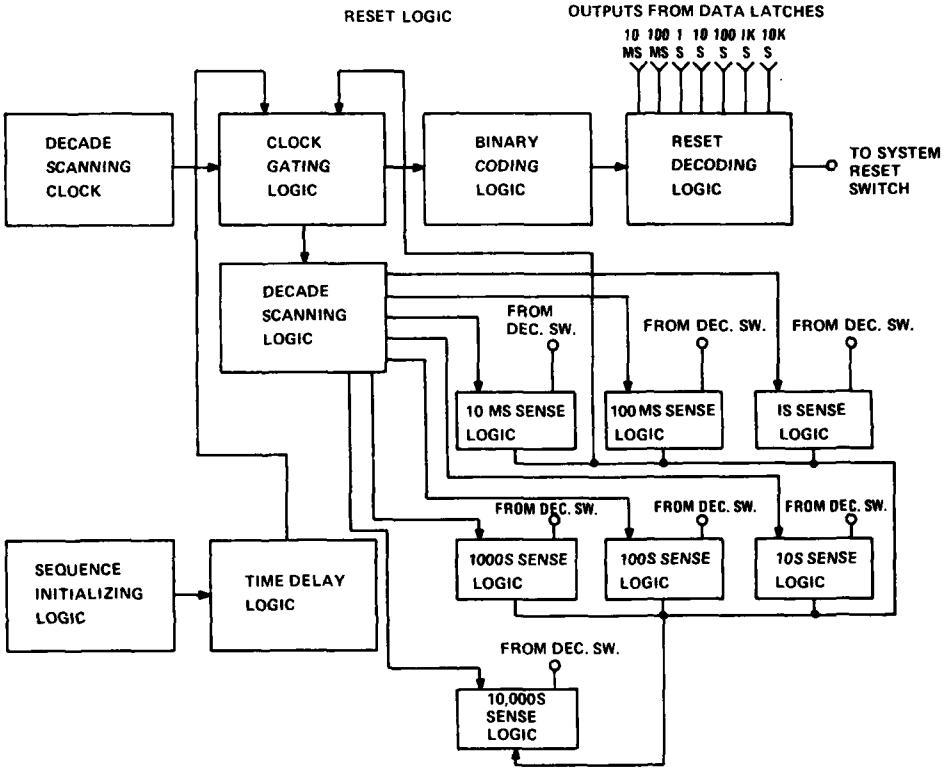


Fig. IV-11 - Reset logic.

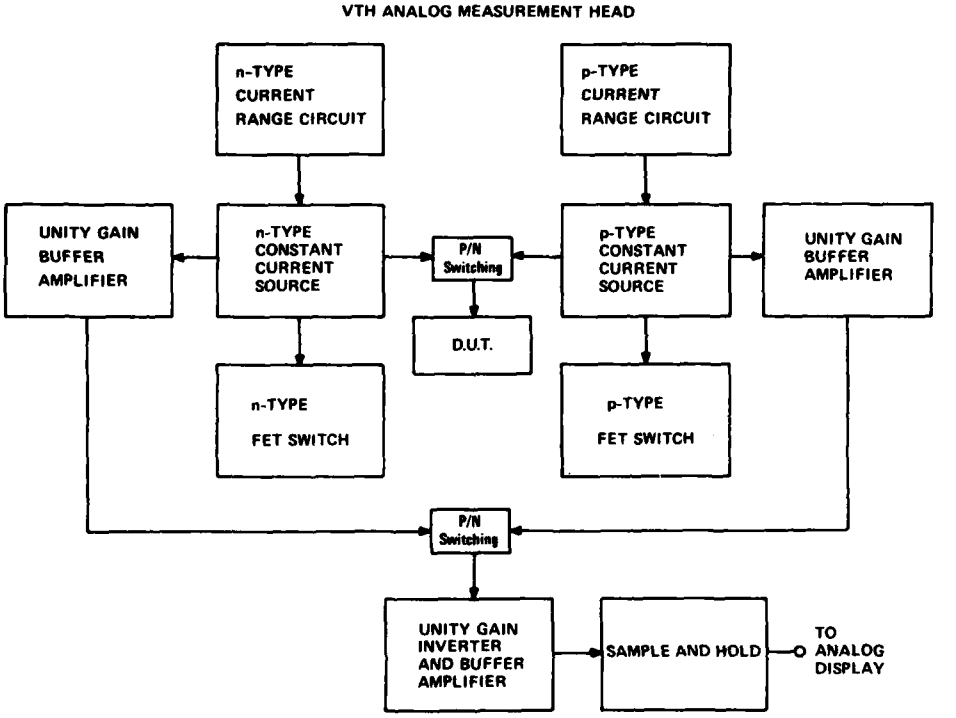


Fig. IV-12 - V_{TH} analog measurement head.

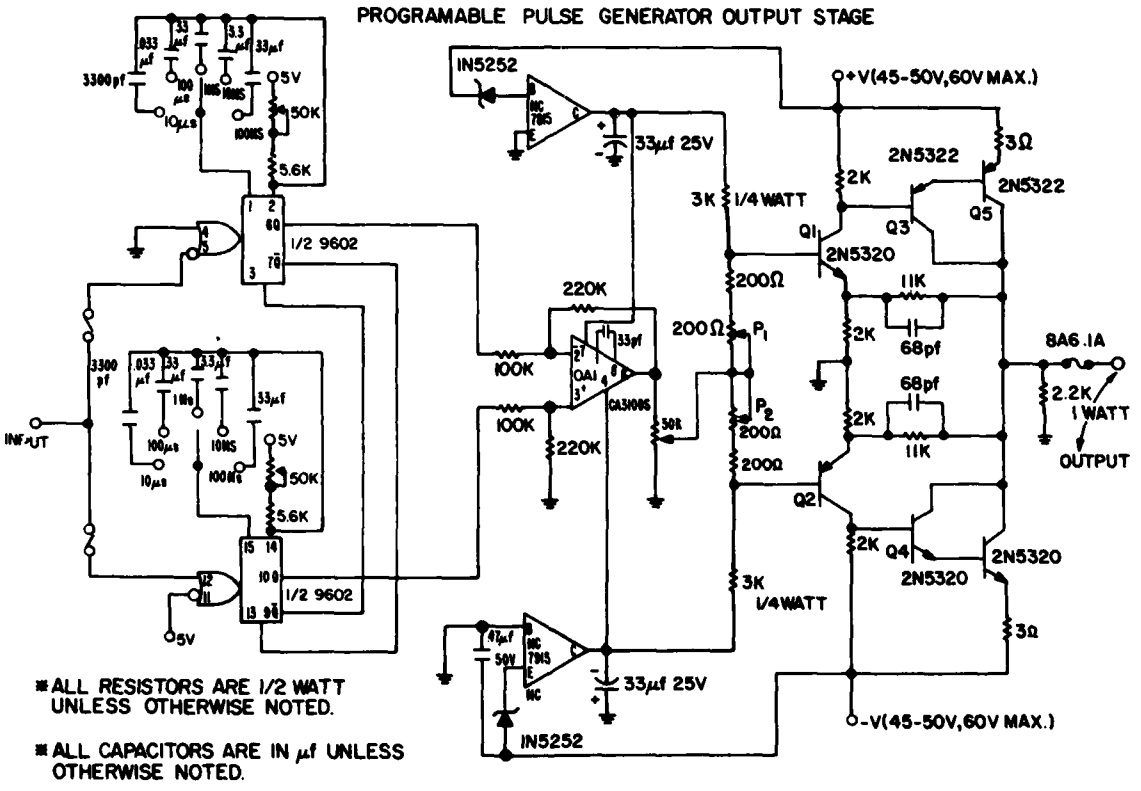
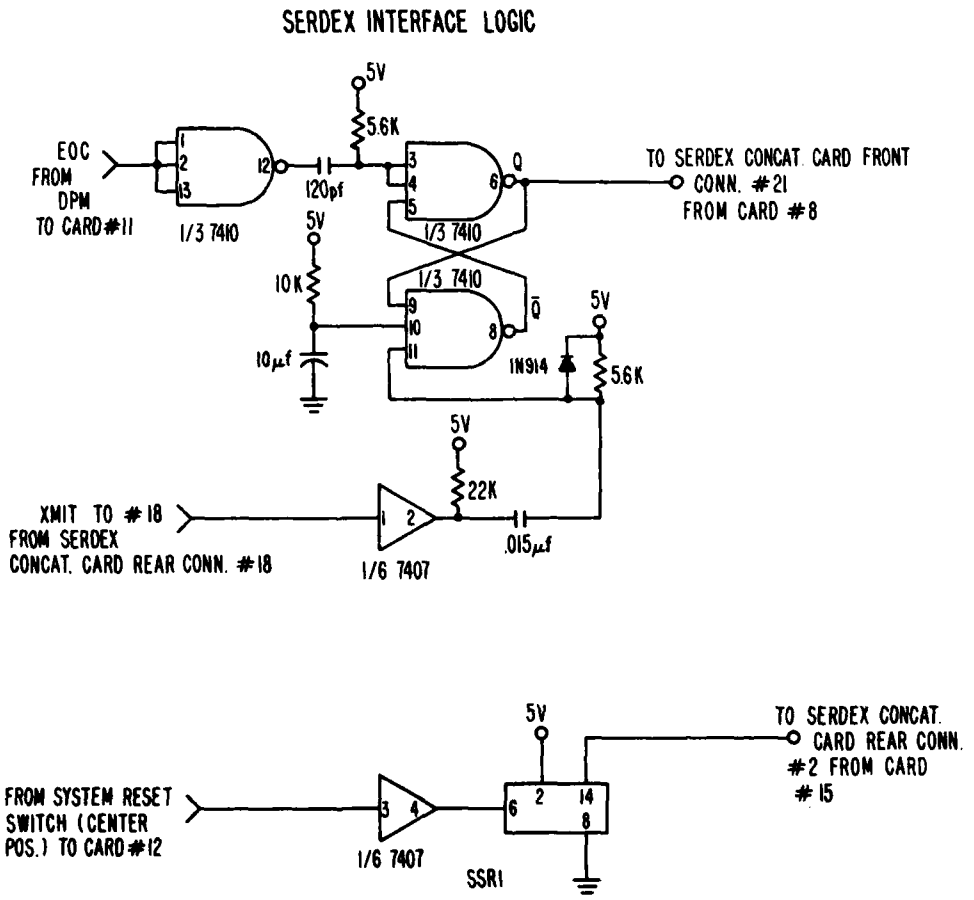


Fig. IV-13 - Programmable pulse generator output stage.



* SSR1 IS A TELEDYNE RELAY #640-1

Fig. IV-14 - SERDEX interface logic.

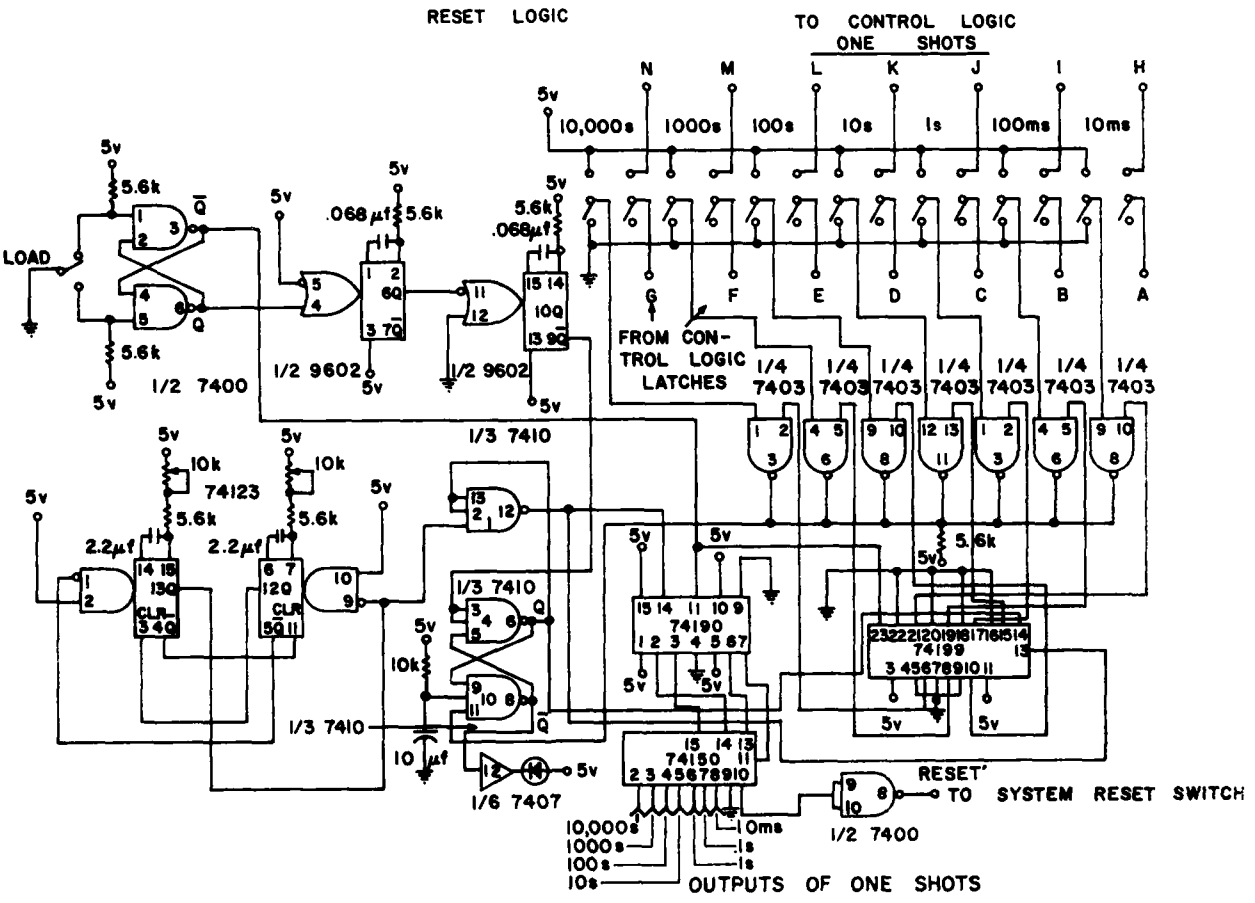


Fig. IV-15 - Reset logic.

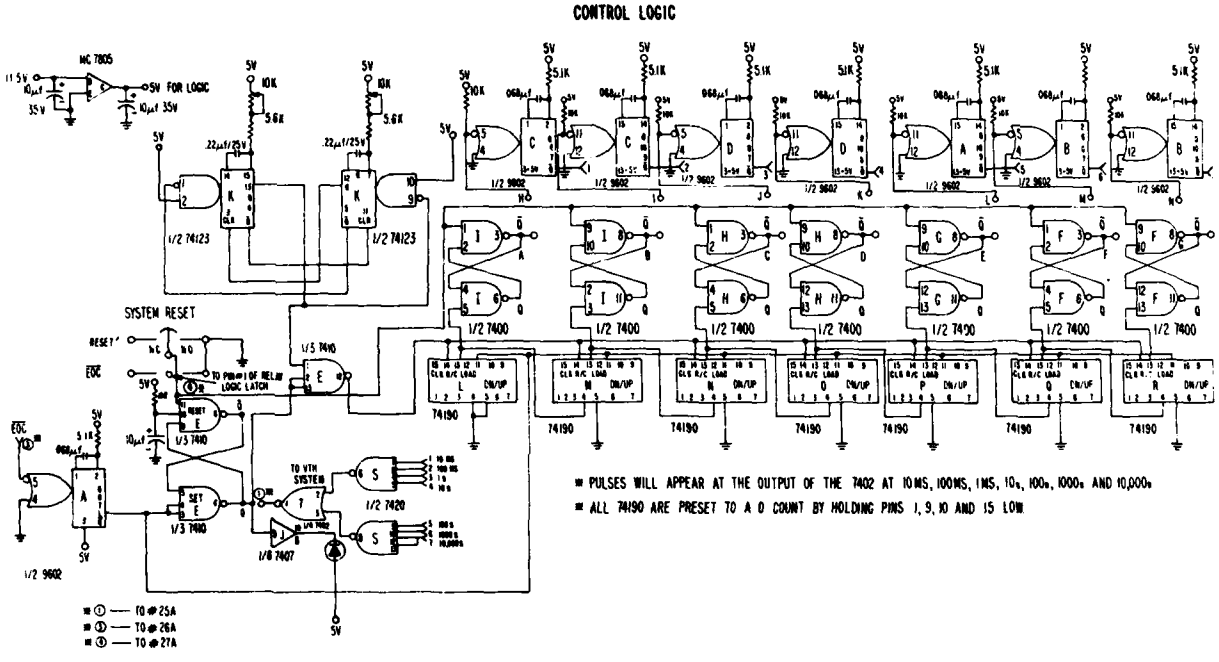


Fig. IV-16 - Control logic.

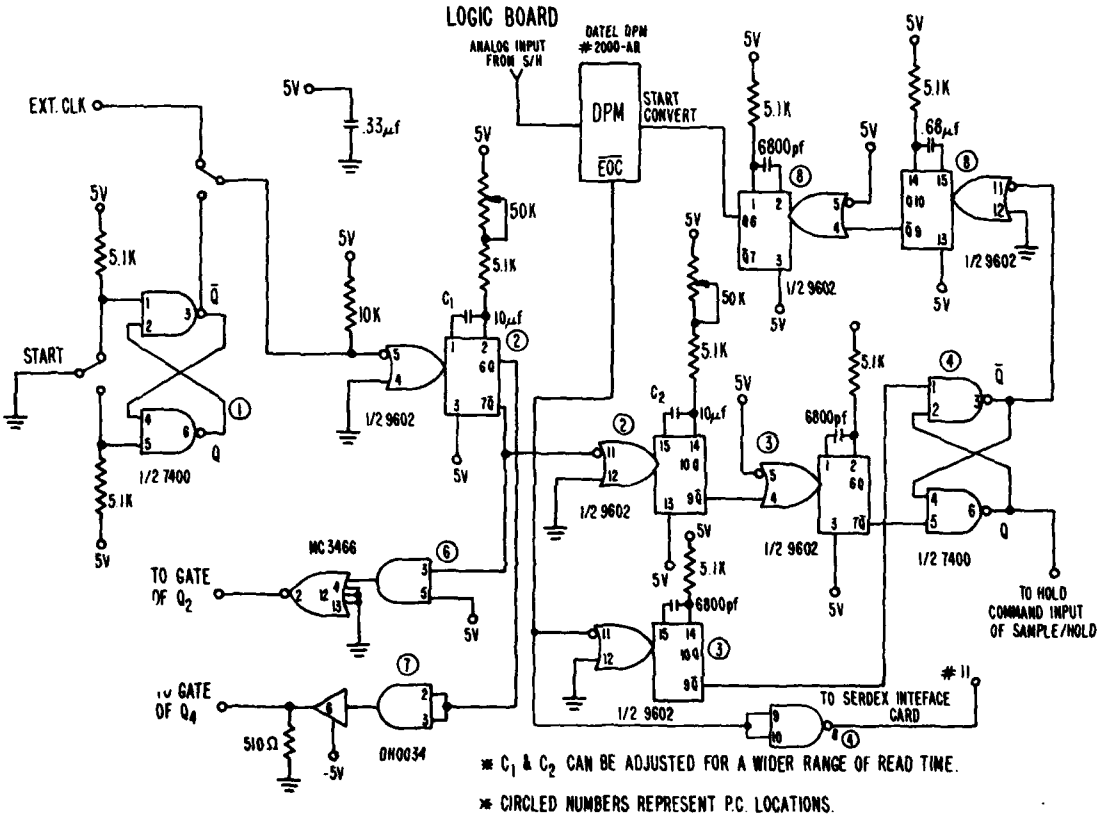


Fig. IV-17 - Logic board.

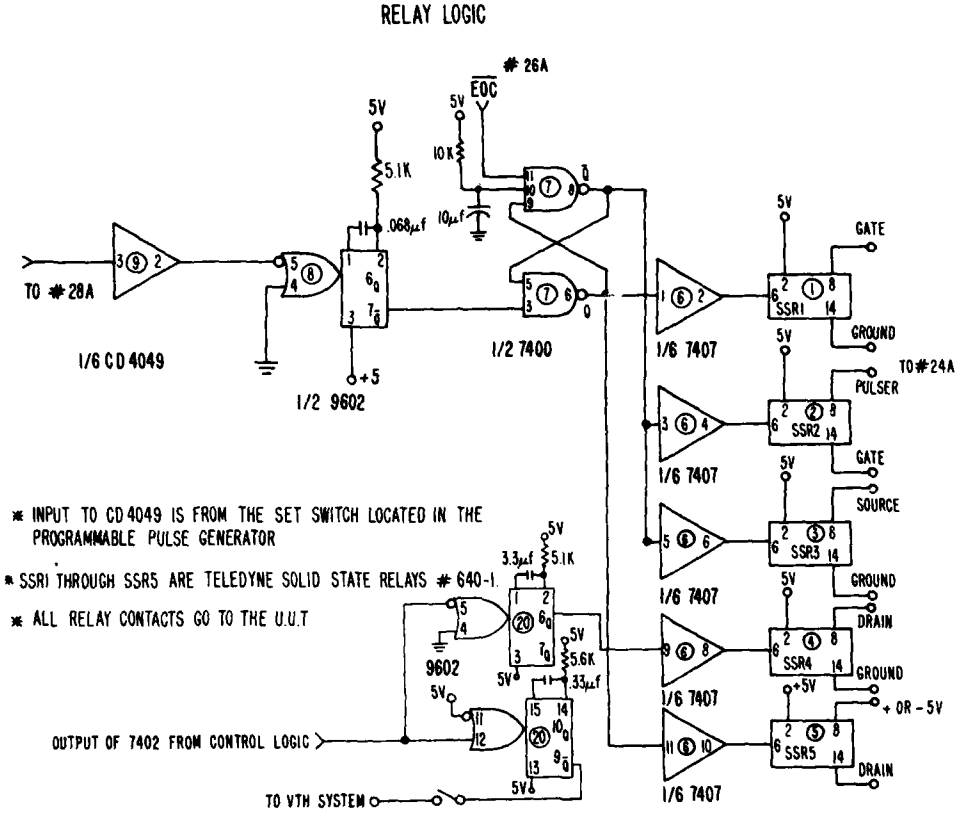


Fig. IV-18 - Relay logic.

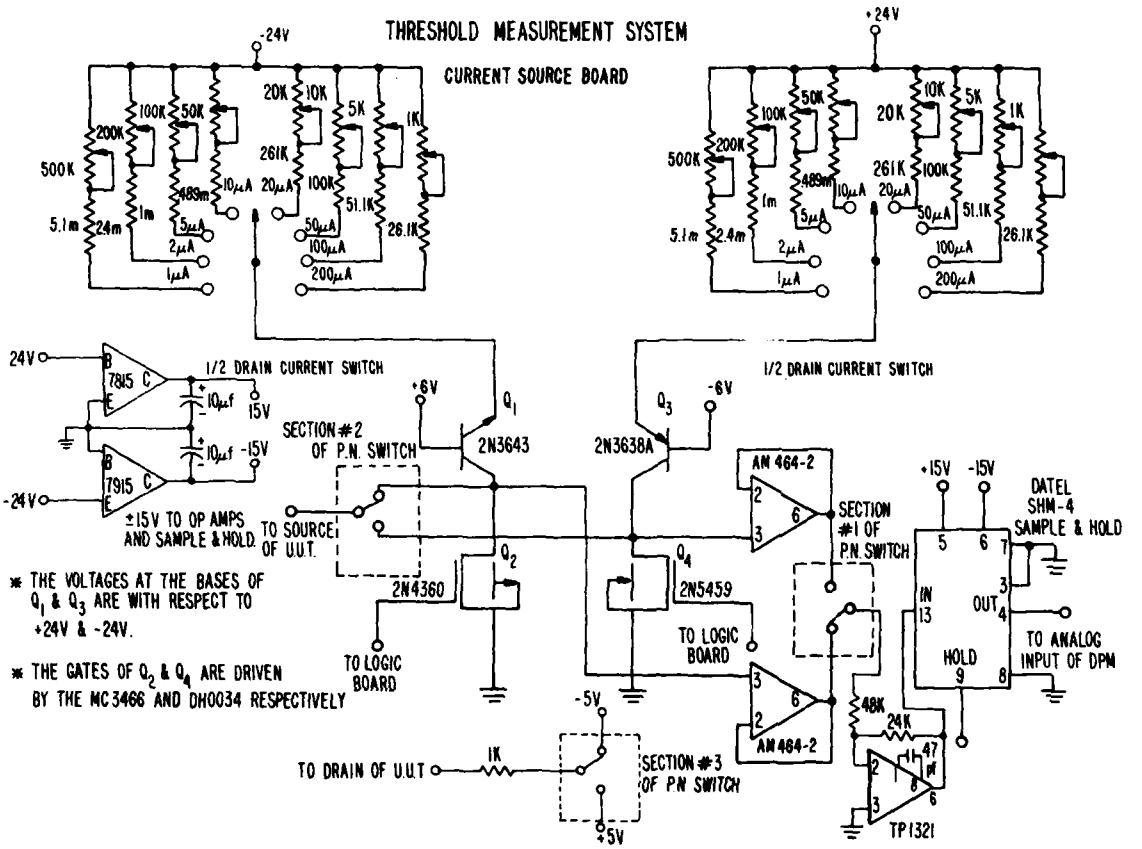


Fig. IV-19 - Threshold measurement system.

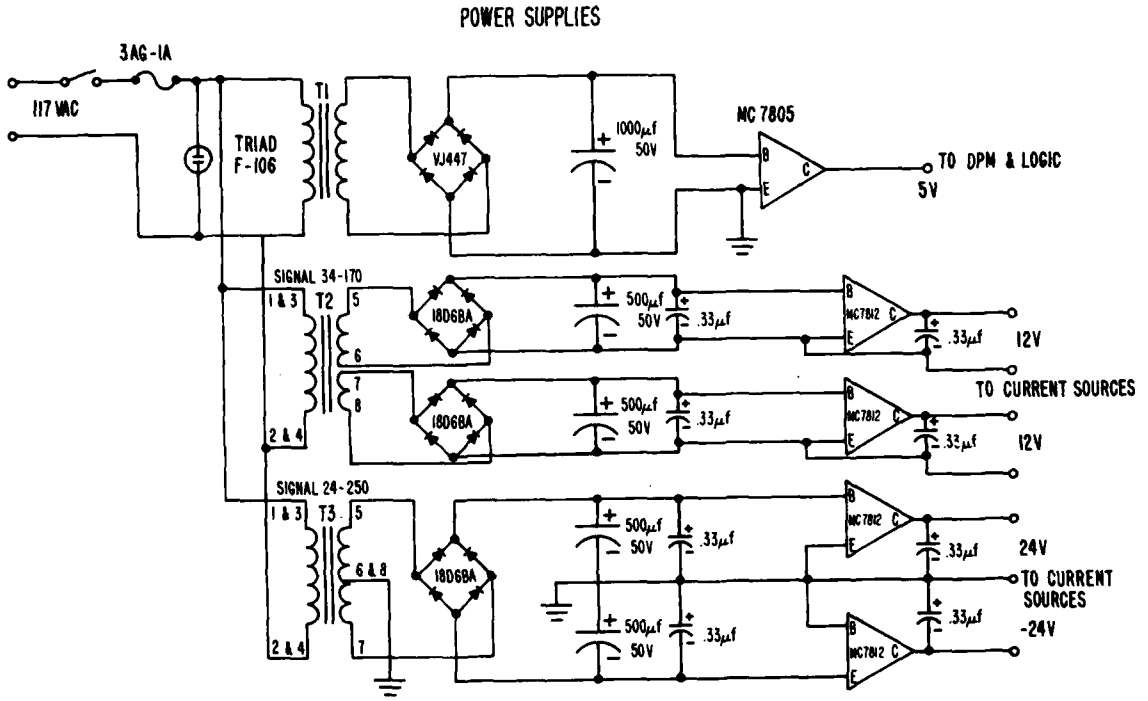


Fig. IV-20 - Power supplies.

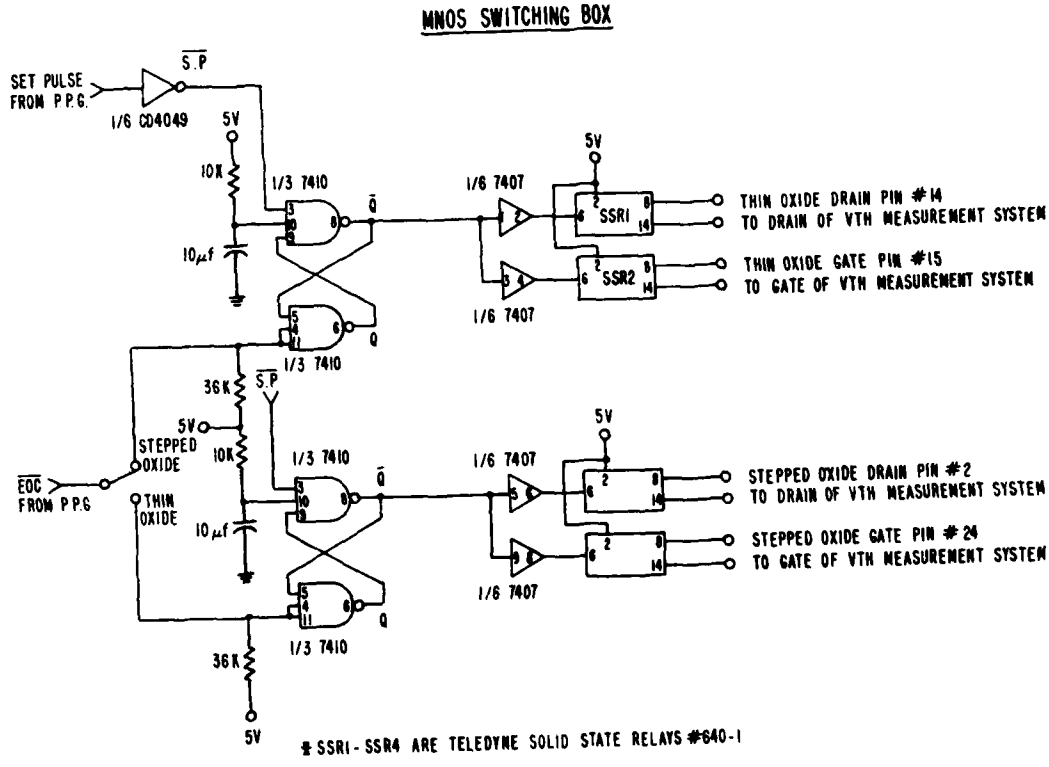


Fig. IV-21 - MNOS switching box.

Table IV-1 - Resistors Used for Calibration and Linearity

Expected Reading	Current Scales							
	1 μa	2 μa	5 μa	10 μa	20 μa	50 μa	100 μa	200 μa
100 mv	100K	49.9K	20K	10K	5.1K	2K	1K	511 Ω
200 mv	200K	100K	38.3K	20K	10K	3.83K	2K	1K
500 mv	499K	261K	100K	49.9K	26.1K	10K	5.1K	2.61K
1v	1m	499K	200K	100K	49.9K	20K	10K	5.1K
2v	2m	1m	383K	200K	100K	38.3K	20K	10K
5v	5.74m	2.61m	1m	499K	261K	100K	49.9K	26.1K
10v	10m	5.74m	2m	1m	499K	200K	100K	49.9K
15v	15.74m	7.66m	3.16m	1.5m	750K	301K	147K	75K

Table - IV-2

MEASURED VALUES OF CALIBRATION RESISTORS

R	V	I	Rm
511Ω	8V	15.5ma	516Ω
1K	.5V	490ma	1.02K
2K	.4V	.198ma	2.02K
2.61K	.4V	151μa	2.65K
3.83K	.4V	102μa	3.92K
5.11K	.4V	77μa	5.19K
10K	.8V	79μa	10.12K
20K	1.6V	78.5μa	20.4K
26.1K	1.6V	61μa	26.2K
38.3K	3.2V	83μa	38.55K
49.9K	4V	79.5μa	50.3K
75K	5V	66μa	75.76K
100K	5V	49.5μa	101K
147K	6V	40.5μa	148.1K
200K	8V	40μa	200K
261K	8V	30.5μa	262.3K
301K	8V	26.5μa	301.9K
383K	8V	20.8μa	384.6K
499K	5.1V	10μa	500K
750K	8V	10.6μa	755K
1m	8V	8μa	1m
1.5m	8V	5.3μa	1.51m
1.25m	8V	4μa	2m
2.61m	8V	31μa	2.58m
3.16m	8V	26μa	3.08m
4.74m	8V	1.68μa	4.761m
7.66m	8V	1.04μ	7.65m
10m	8V	.8μa	10m

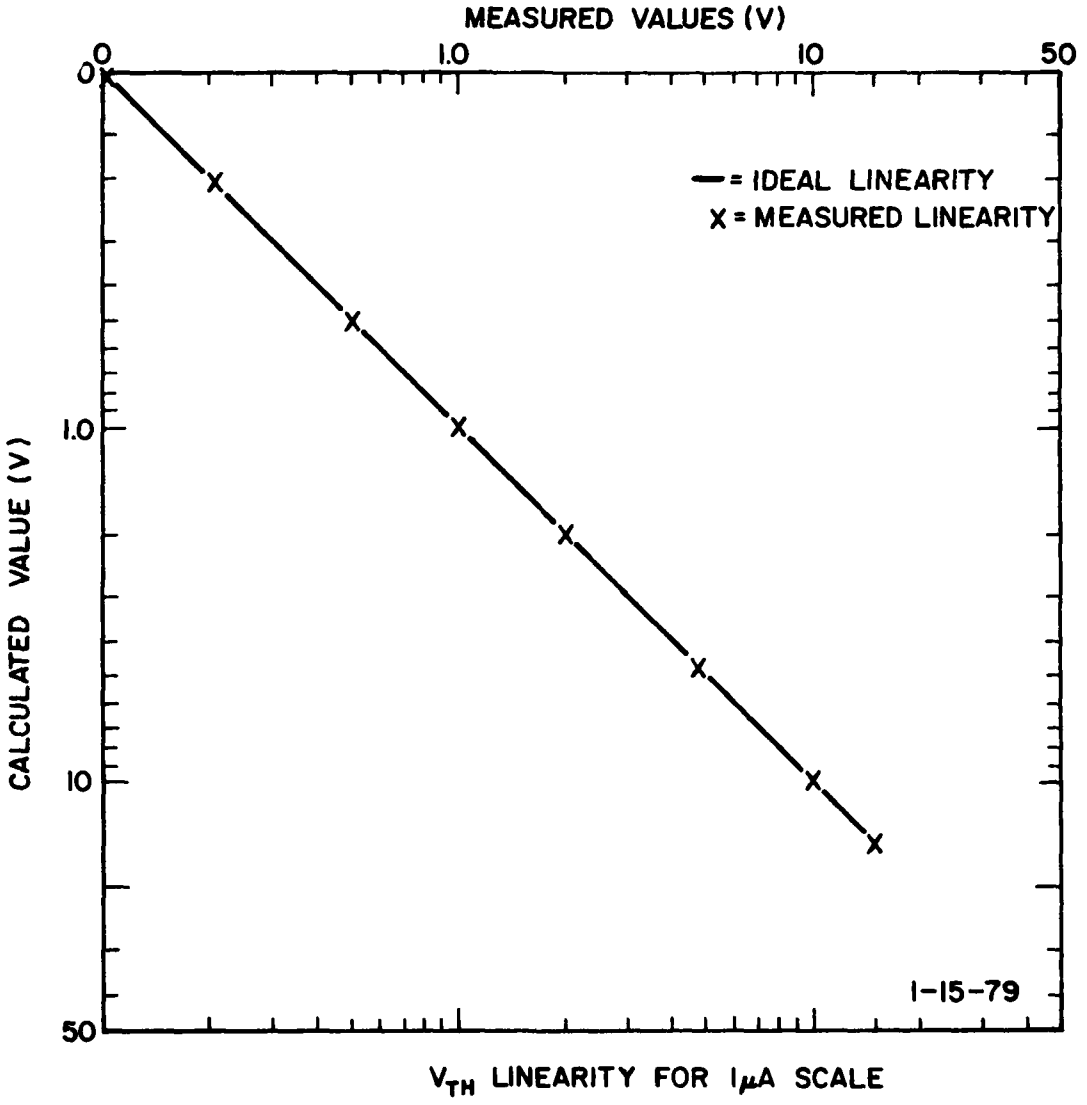


Fig. IV-22 - V_{TH} linearity for 1 microampere scale.

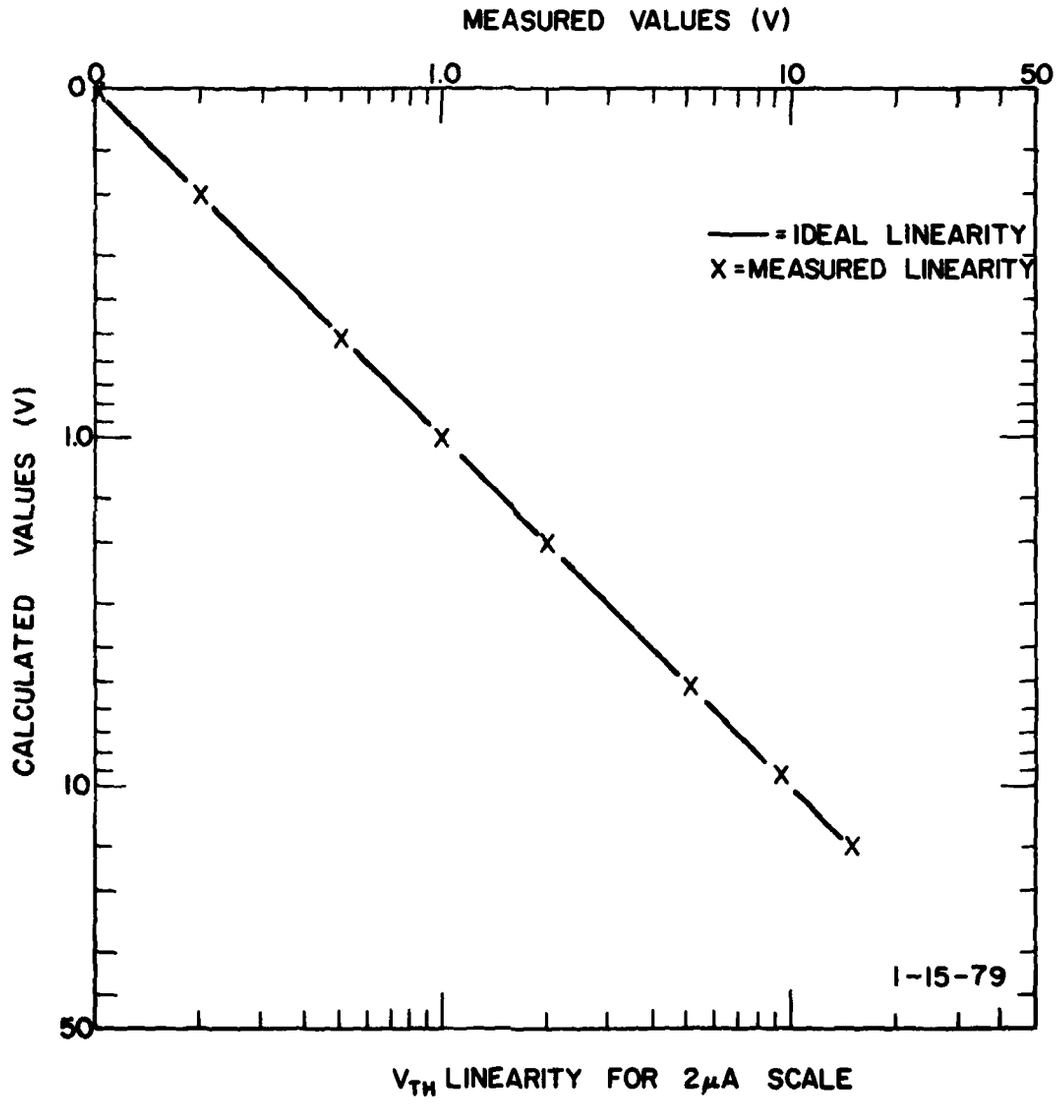


Fig. IV-23 - V_{TH} linearity for 2 microampere scale.

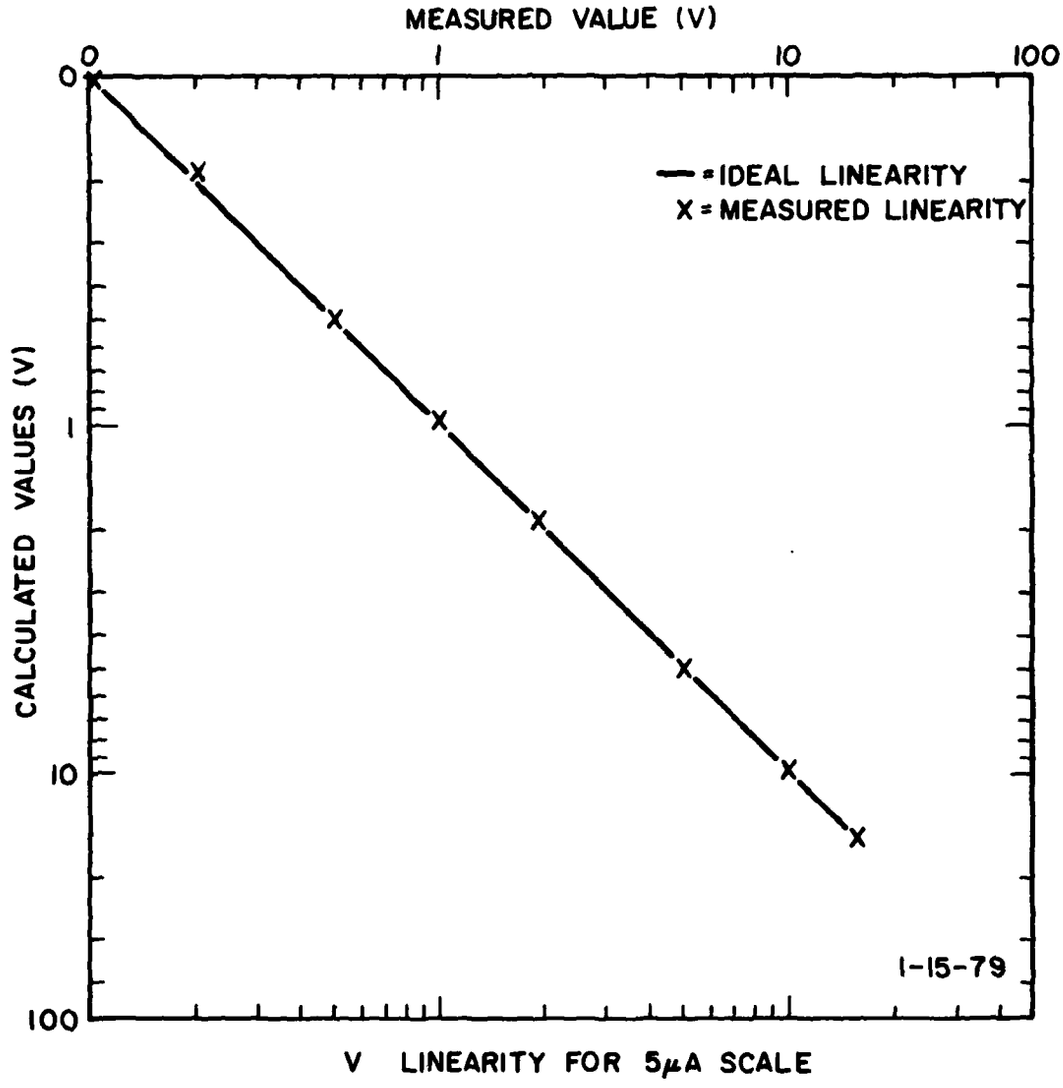


Fig. IV-24 - V_{TH} linearity for 5 microampere scale.

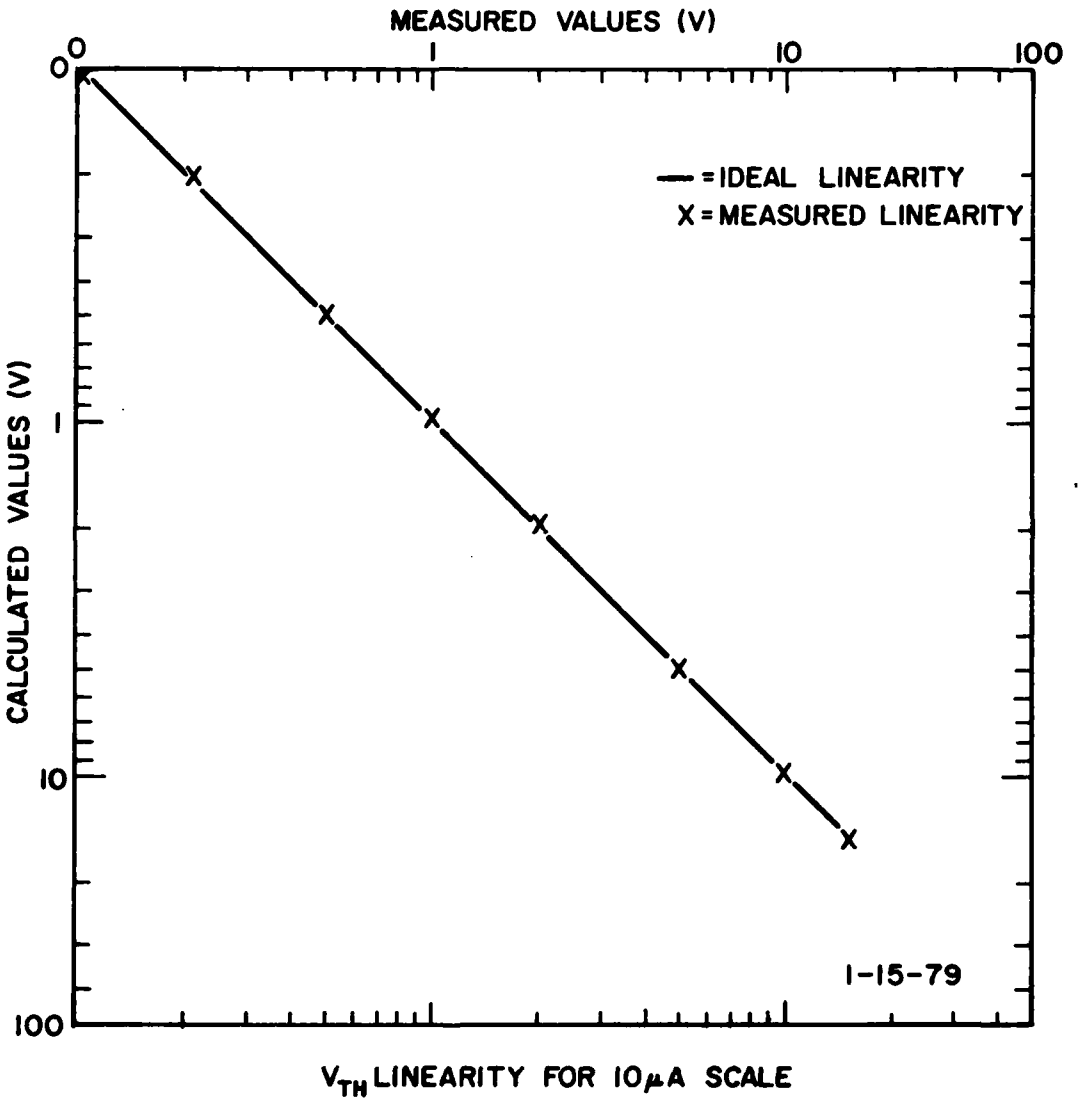


Fig. IV-25 - V_{TH} linearity for 10 microampere scale.

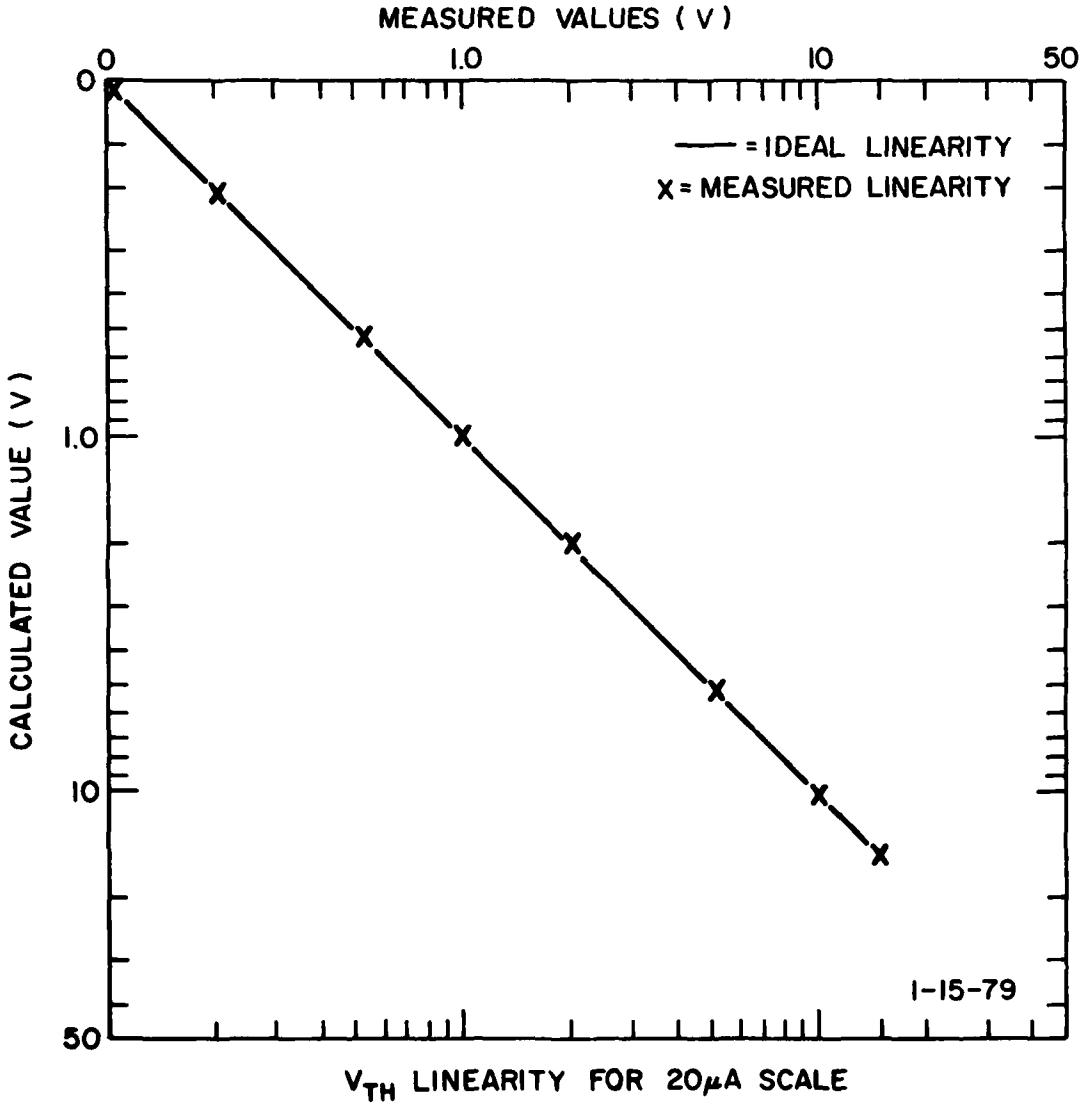


Fig. IV-26 - V_{TH} linearity for 20 microampere scale.

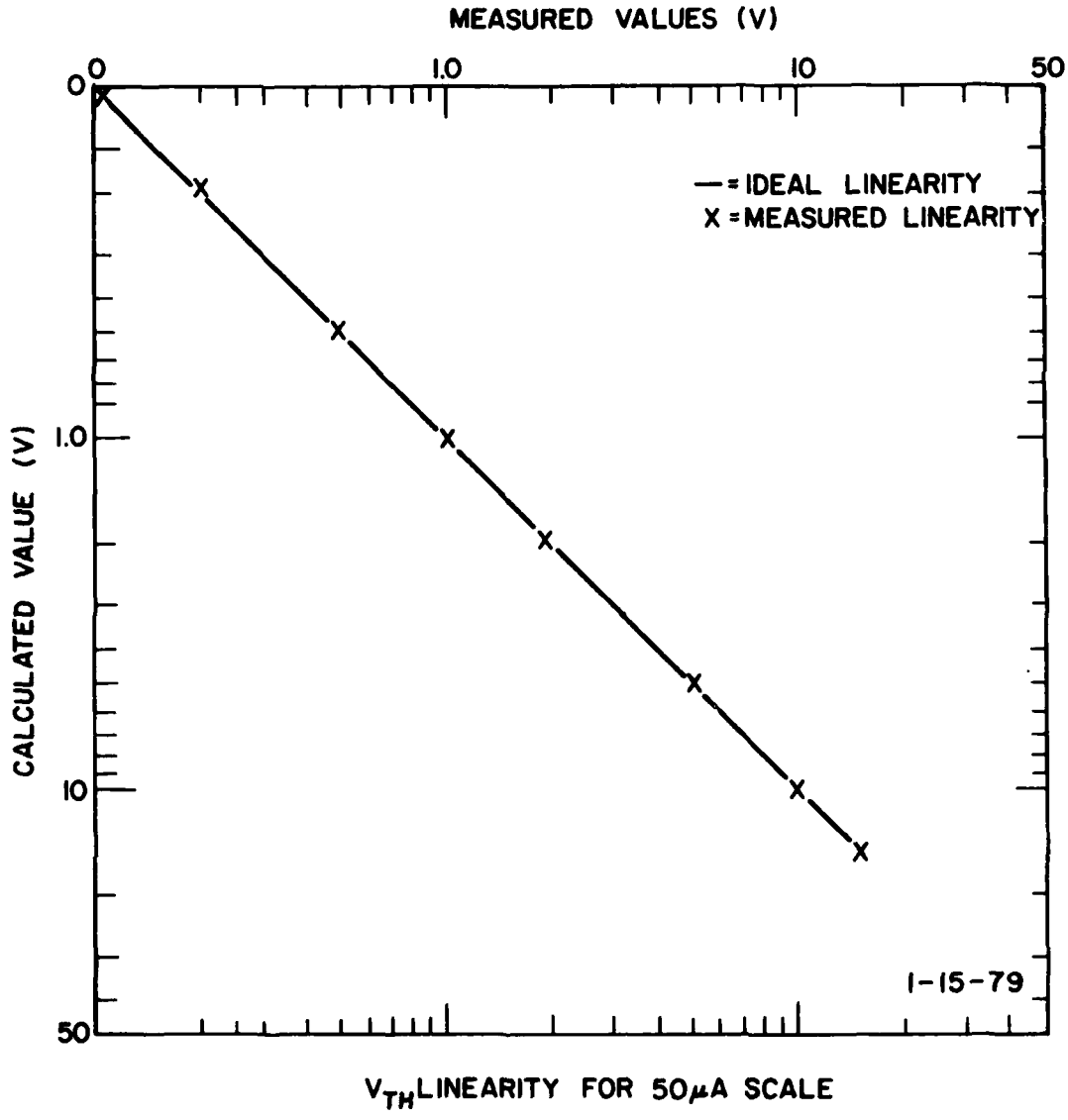


Fig. IV-27 - V_{TH} linearity for 50 microampere scale.

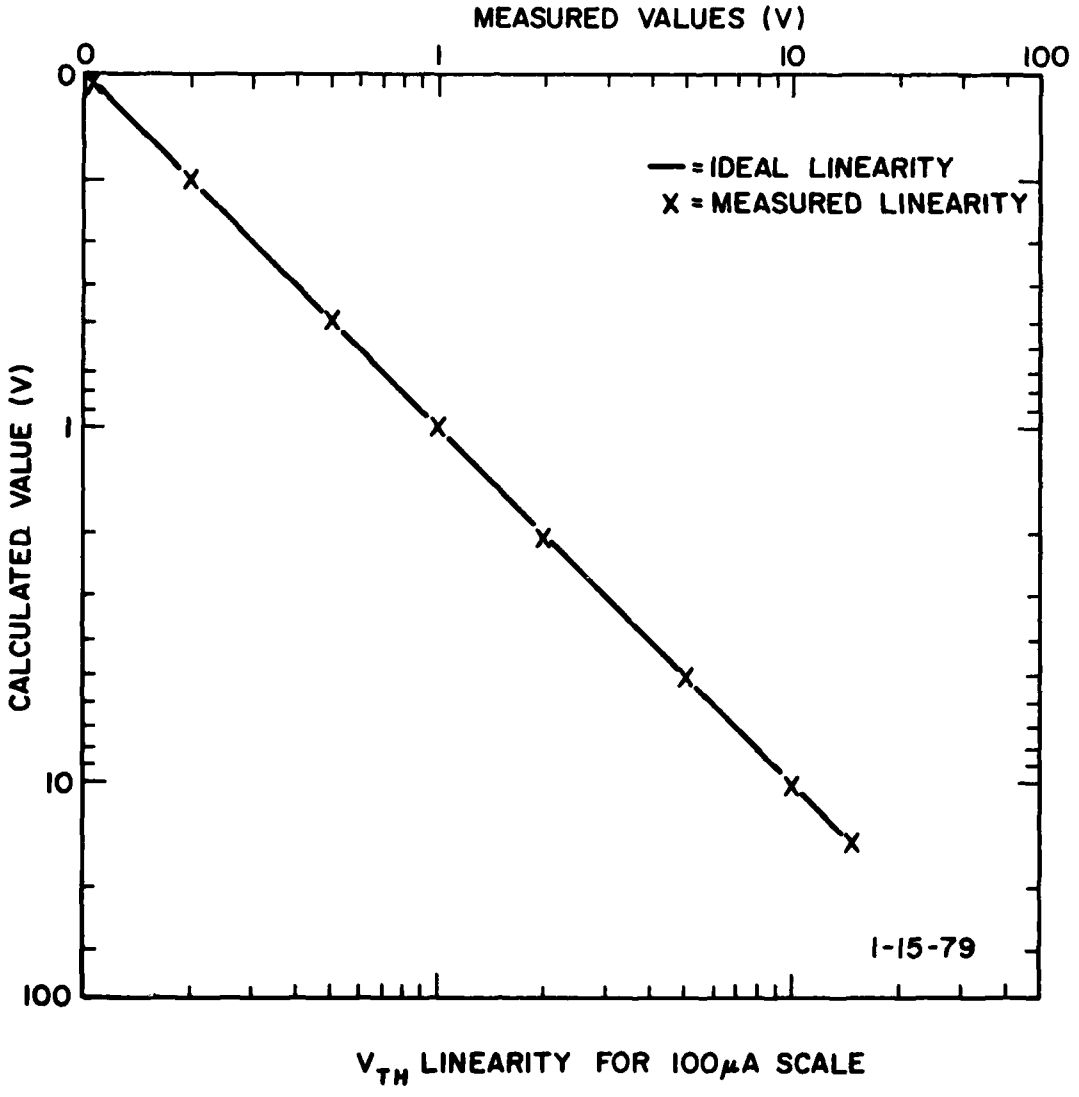


Fig. IV-28 - V_{TH} linearity for 100 microampere scale.

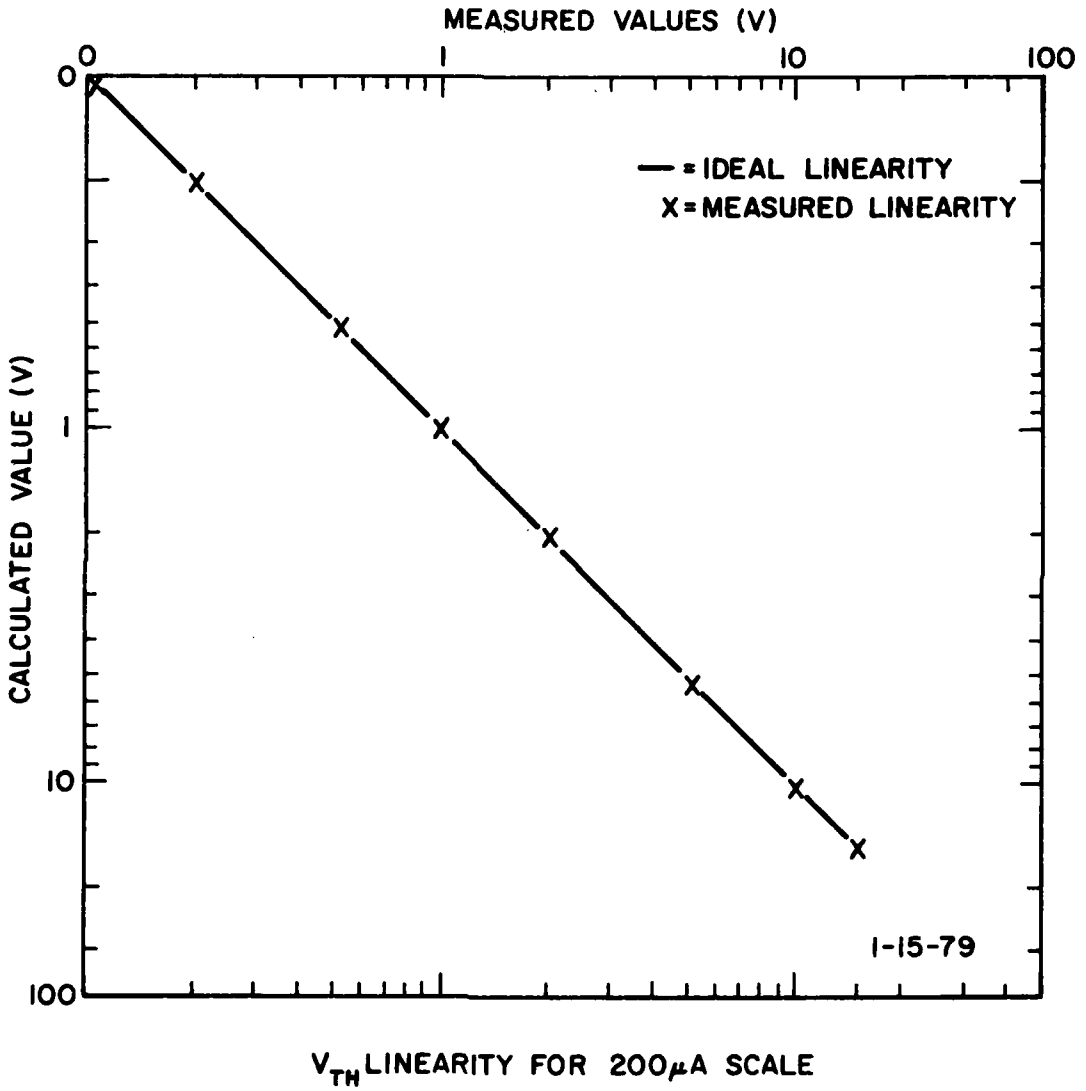
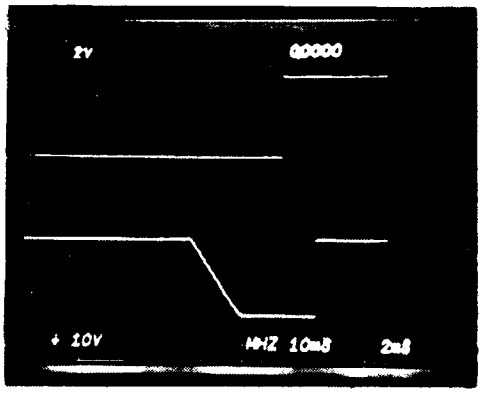


Fig. IV-29 - V_{TH} linearity for 200 microampere scale.

VTH TIMING



TOP TRACE

VERT. = 2V/DIV.
HOR. = 2 ms/DIV.

BOTTOM TRACE

VERT = 10V/DIV.
HOR = 2ms/DIV.

(1) BOTTOM TRACE SHOWS OPEN CIRCUIT READ PULSE AFTER FIRST BUFFER AMPLIFIER WITH ALL CABLING ATTACHED.

(2) TOP TRACE SHOWS WHEN VTH SYSTEM READS THE U.U.T AS DEPICTED BY POSITIONING THE RISING EDGE.

Fig. IV-30 - V_{TH} timing information.

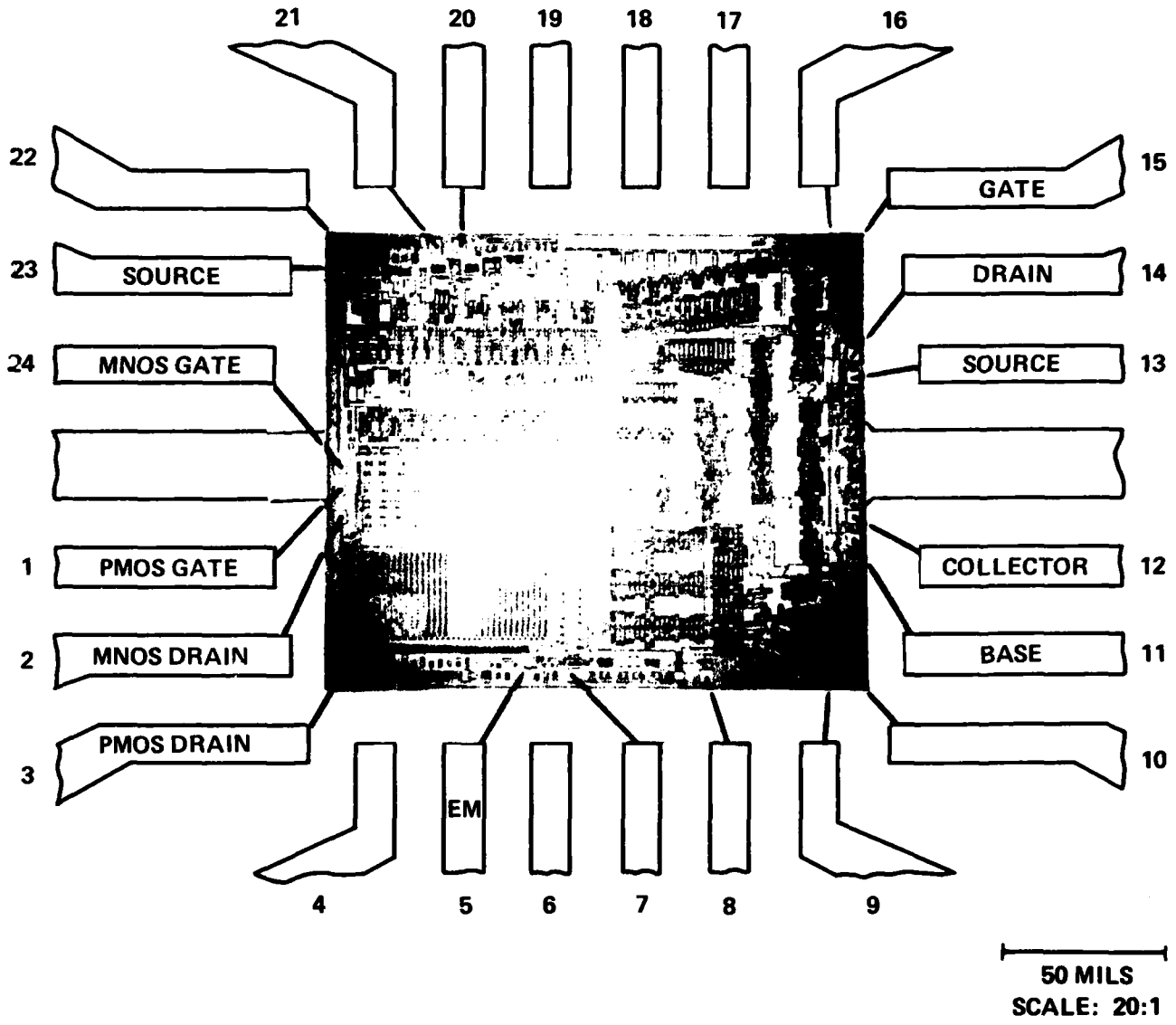


Fig. IV-31 - Photomicrograph and bond-out diagram of test key, TA10306: 24-lead dual-in-line ceramic; pellet size, 200 x 170 mils; frame, NR496.

Table IV-3 - Initial V_{TH} of Units 1 through 124

Unit	V_{TH}- Stepped Oxide	V_{TH}- Thin Oxide
	LOT NO. 2A	
1	-4.26v	-3.36v
2	-2.14v	-3.21v
3	-3.06v	-2.98v
4	-2.22v	-2.24v
5	-2.52v	-2.46v
6	-2.40v	-3.94v
7	-2.81V	-6.36v
8	-3.16v	-3.60v
9	-3.38v	-3.30v
10	-3.60v	-3.46v
11	-2.46v	-3.28v
12	-2.44v	-3.40v
13	-4.16v	-3.32v
14	-1.64v	-3.38v
15	-2.38v	-3.04v
16	-3.28v	-2.64v
17	-3.70v	-3 94v
18	-2.30v	-2.52v
19	-2.40v	-2.38v
20	-3.60v	-3.92v
21	-2.44v	-3.38v
22	-3.94v	-2.98v

Table IV-3 - Initial V_{TH} of Units 1 through 124

Unit	V_{TH}- Stepped Oxide	V_{TH}- Thin Oxide
23	-2.20v	-.358v
24	-2.40v	-2.94v
25	-2.34v	-3.40v
26	-2.86v	-3.63v
27	-3.12v	-1.93v
28	-2.29v	-3.34v
29	-2.48v	-3.11v
30	-2.34v	-.048v
31	-7.85v	-3.94v
32	-5.59v	-3.49v
33	-13.00v	-4.79v
34	-2.35v	-3.46v
35	-2.39v	-3.72v
36	-2.38v	-3.26v
	LOT NO. 10A	
37	-3.16v	-3.71v
38	-2.83v	-3.69v
39	-3.56v	-3.66v
40	-3.43v	-3.37v
41	-2.75v	-3.55v
42	-2.94v	-4.24v
43	-3.40v	-4.57v
44	-2.62v	-3.64v

Table IV-3 - Initial V_{TH} of Units 1 through 124

Unit	V_{TH}- Stepped Oxide	V_{TH}- Thin Oxide
45	-2.73v	-3.78v
46	-3.19v	-4.28v
47	-4.09v	-3.94v
48	-2.89v	-3.78v
49	-4.38v	-3.65v
50	-2.73v	-4.29v
51	-2.67v	-3.65v
52	-3.52v	-1.78v
	LOT NO. 13A	
53	-3.03v	-6.17v
54	-3.14v	-.0075v
55	-6.06v	-3.51v
56	-0053v	-4.81v
57	-2.83v	-3.23v
58	-3.26v	-3.59v
59	-3.12v	-3.84v
60	-3.06v	-.0057v
61	-3.07v	-4.59v
62	-3.95v	-3.82v
63	-13.00v	-3.48v
64	-3.10v	-3.89v
65	-2.83v	-2.33v

Table IV-3 - Initial V_{TH} of Units 1 through 124

Unit	V_{TH} - Stepped Oxide	V_{TH} - Thin Oxide
66	-3.72v	-3.75v
67	-13.00v	-.045v
68	-2.44v	-1.21v
69	-2.93v	-3.58v
70	-2.60v	-3.23v
71	-2.65v	-3.76v
72	-3.50v	-3.80v
73	-3.17v	-3.71v
74	-3.23v	-3.74v
75	-3.12v	-3.73v
76	-3.28v	-3.82v
77	-3.93v	-3.74v
78	-3.14v	-3.71v
79	-3.05v	-3.67v
80	-3.01v	-3.69v
81	-3.12v	-3.54v
82	-2.93v	-.049v
83	-3.24v	-3.32v
84	-4.10v	-0.12v
85	-13.00v	-13.00v
86	-2.94v	-.053v
87	-3.97v	-4.21v

Table IV-3 - Initial V_{TH} of Units 1 through 124

Unit	V_{TH}- Stepped Oxide	V_{TH}- Thin Oxide
	LOT NO. 17	
88	-10.00v	-13.00v
89	-3.02v	-2.84v
90	-2.27v	-2.82v
91	-3.08v	-2.94v
92	-2.72v	-2.85v
93	-3.27v	-2.71v
94	-2.32v	-3.20v
95	-3.10v	-3.14v
96	-4.27v	-1.07v
97	-2.23v	-2.78v
98	-2.31v	-2.47v
99	-3.22v	-2.74v
100	-1.92v	-3.06v
101	-3.27v	-3.26v
102	-2.27v	-2.77v
103	-2.28v	-3.04v
104	-2.95v	-2.97v
105	-2.27v	-2.83v
106	-2.16v	-2.80v
107	-2.89v	-2.87v
108	-2.27v	-2.84v
109	-2.68v	-2.82v

Table IV-3 - Initial V_{TH} of Units 1 through 124

Unit	V_{TH}- Stepped Oxide	V_{TH}- Thin Oxide
110	-.546v	-2.90v
111	-2.95v	-2.85v
112	-2.89v	-2.87v
113	-2.31v	-2.78v
114	-2.60v	-1.17v
115	-2.29v	-3.08v
116	-2.28v	-2.92v
117	-2.06v	-3.16v
118	-2.25v	-2.26v
119	-2.91v	-3.02v
120	-2.28v	-2.84v
121	-2.93v	-2.78v
122	-2.28v	-.303v
123	-.052v	-2.87v
124	-2.98v	-3.10v
	LOT NO. 18	
1	-4.10v	-2.45 v
2	+.050v	+.100 v
3	-3.90v	-2.45 v
4	-4.11v	-2.32 v
5	+1.34v	-3.56 v

Table IV-3 - Initial V_{TH} of Units 1 through 124

Unit	V_{TH}- Stepped Oxide	V_{TH}- Thin Oxide
6	-3.88 v	-2.29 v
7	-3.90 v	-2.12 v
8	-2.33 v	-5.60 v
9	-13.00 v	-4.79 v
10	+5.42 v	-2.28 v
11	-3.84 v	-2.38 v
12	-4.14 v	-5.85 v
13	-13.00 v	-2.39 v
14	-3 48 v	-2.32 v
15	-3.53 v	+.180 v
16	-3.30 v	-2.44 v
17	-3.25 v	-4.39 v
18	+1.80 v	-2.40 v
19	-2.66 v	-6.66 v
20	-5.26 v	-2.32 v
21	-.0545 v	+2.03 v
22	-3.76 v	-2.39 v
23	-3.49 v	-2.55 v

Table IV-4 - Typical Source-To-Drain Breakdown Voltage

Lot	Device	V_{BD} - Volts	
		Thin Oxide	Stepped Oxide
2A	3	-34	-34
	8	-70	-34
	9	-35	
	10	-33	-32
	11	-34	-34
	13	-34	-33
10A	37	-32	-32
	39	-31	-32
	40	-32	-32
	42	-31	-31
	43	-31	-32
	45	-32	-33
13A	53	-28	-29
	55	-28	-30
	66	-28	-30
	72	-32	-30
	73	-29	-28
	87	-28	-28
18	3	-32	-32
	4	-32	-31
	6	-32	-31
	7	-34	-32
	8	-34	-34
	11	-33	-22

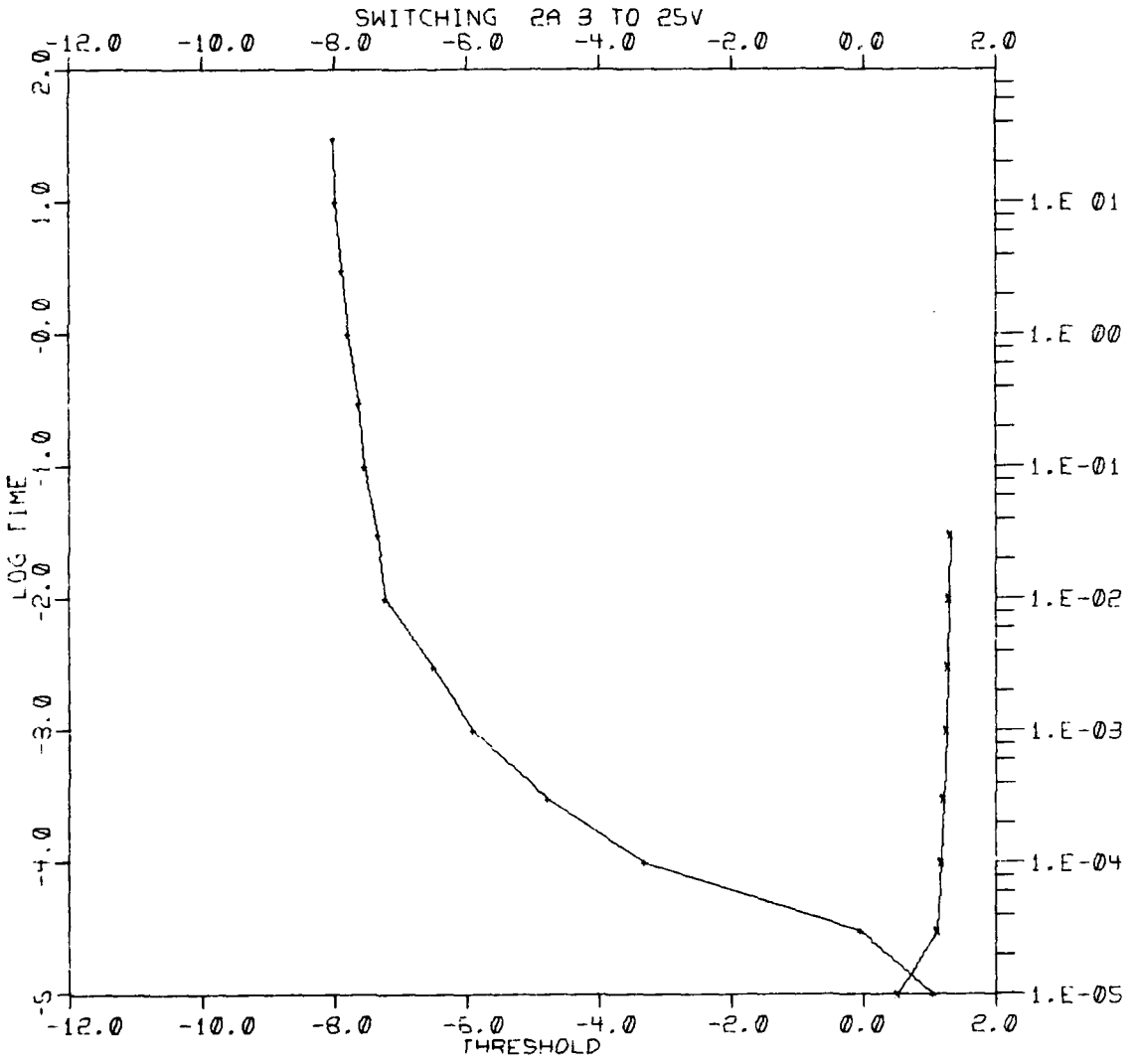

SWITCHING 2A 3 TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-32

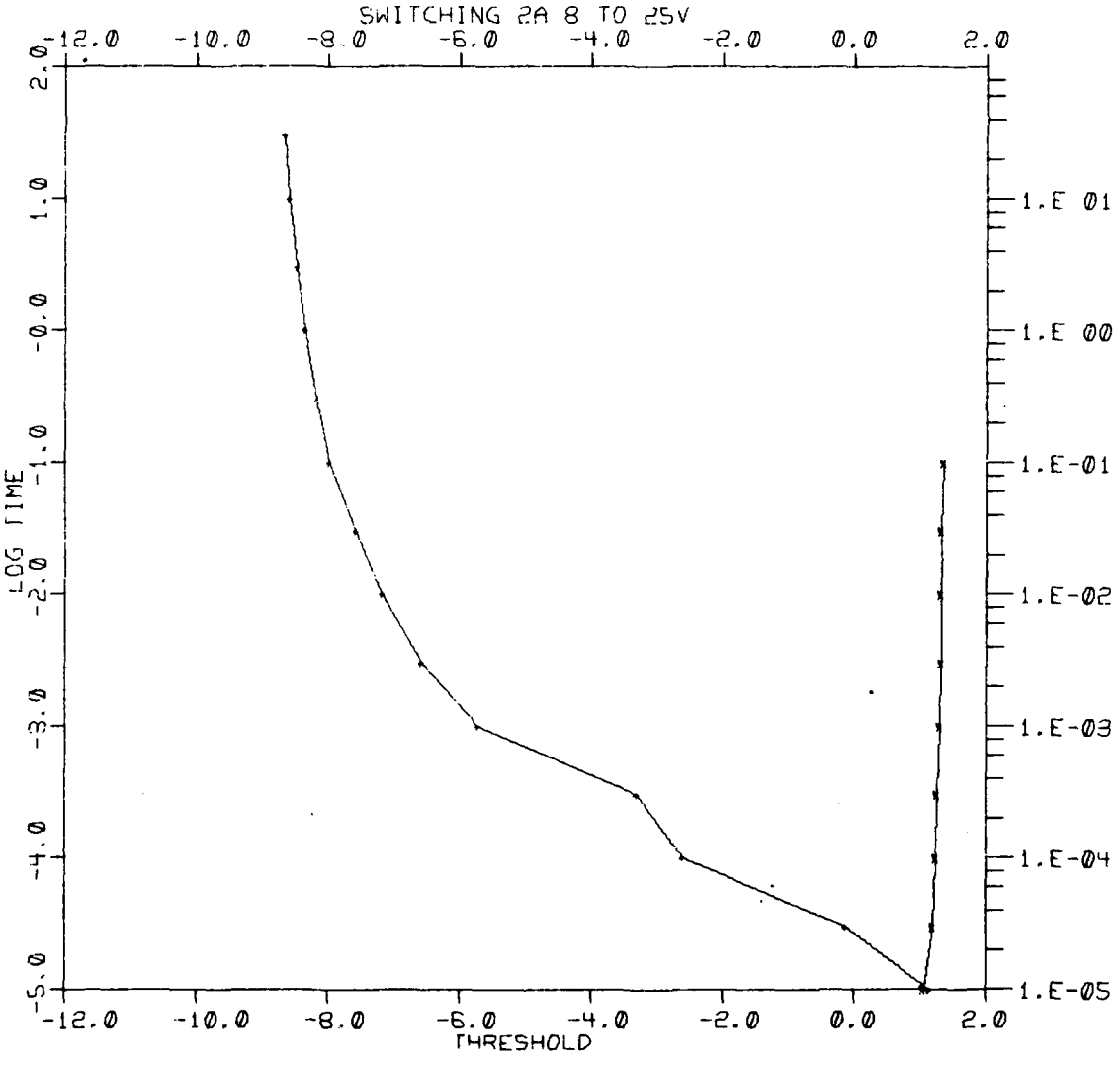

SWITCHING 2A 8 TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-33

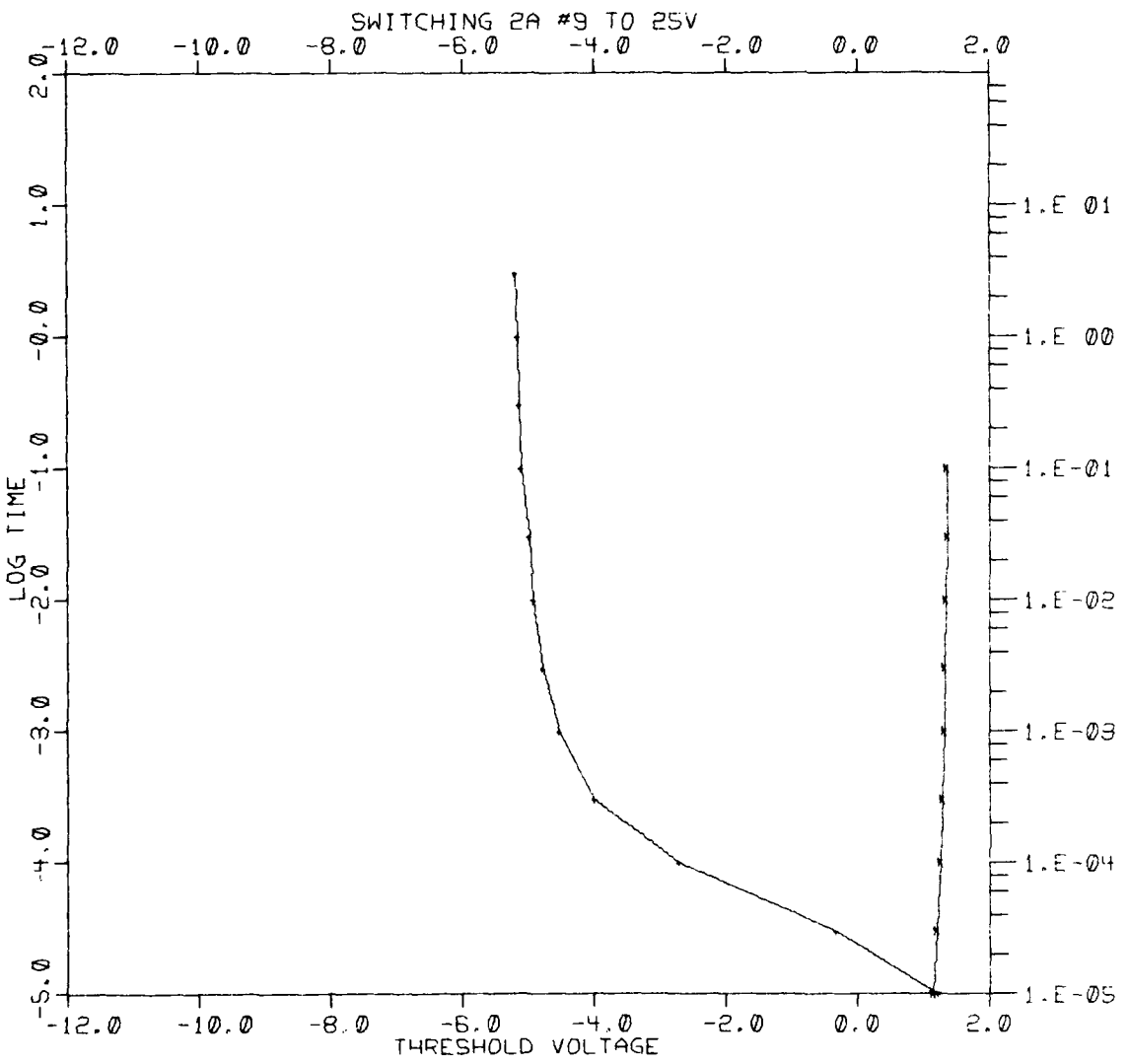
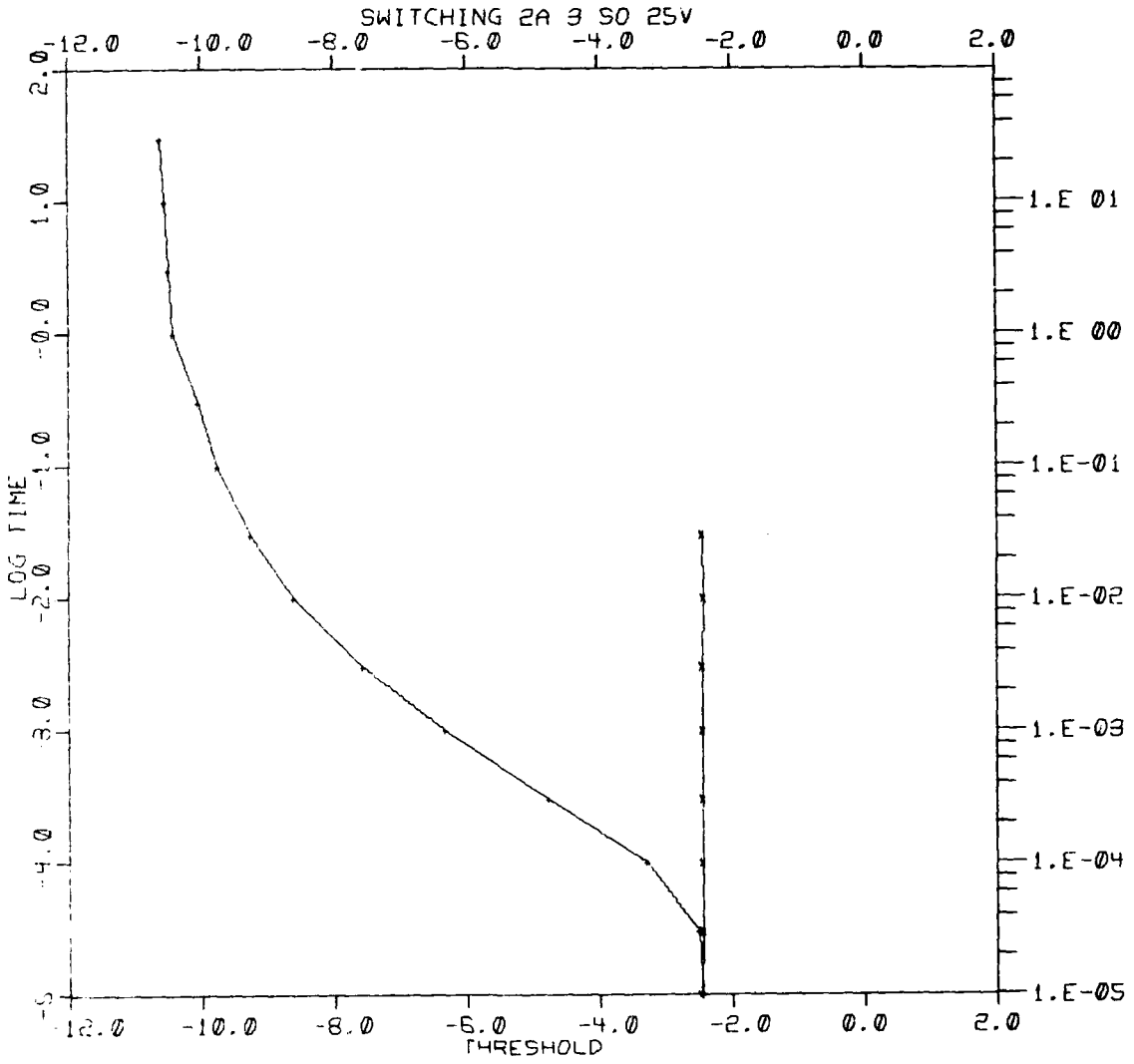

SWITCHING 2A #9 TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-34



Stepped Oxide

Fig. IV-35

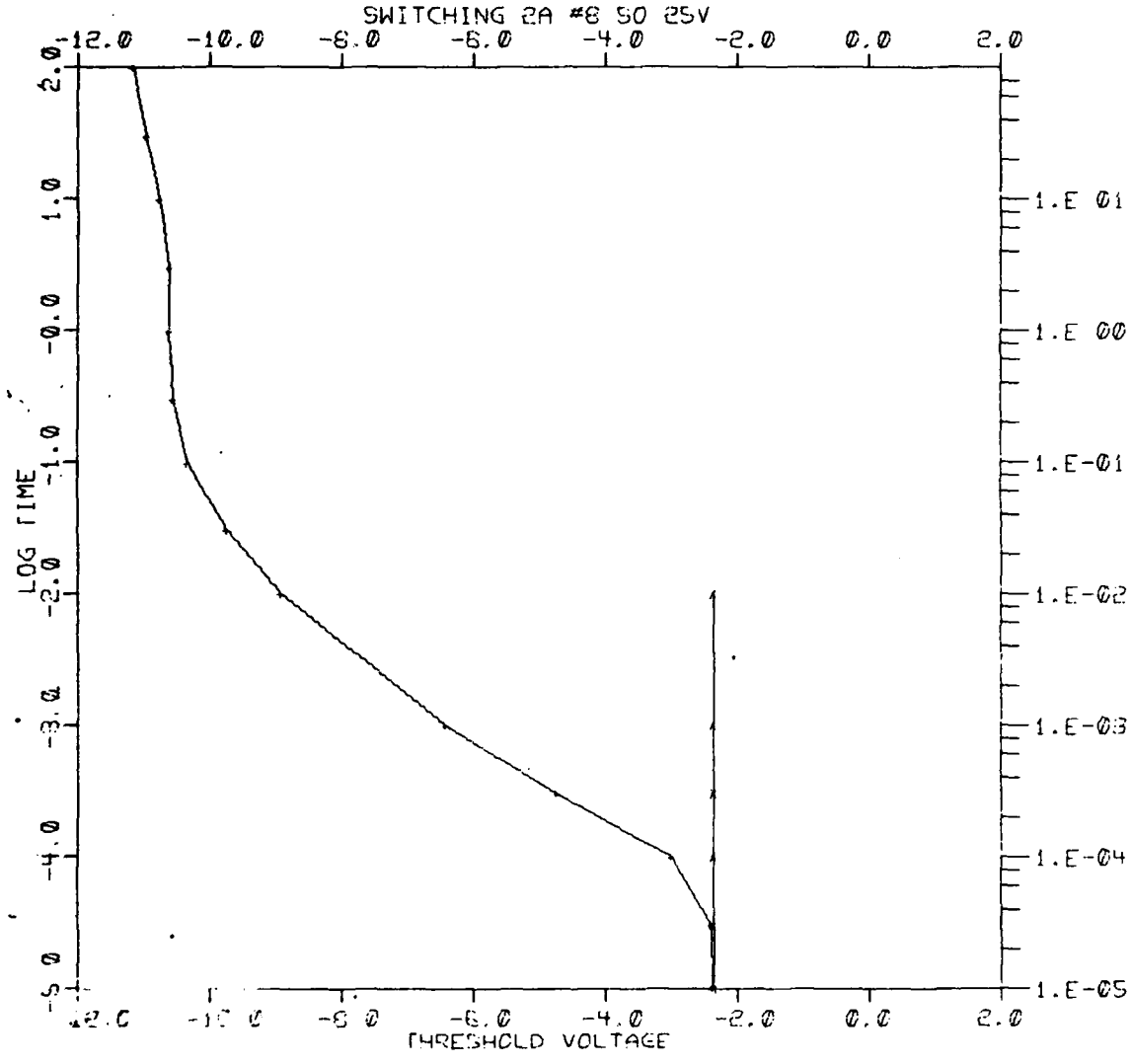

SWITCHING 2A #8 50 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-36

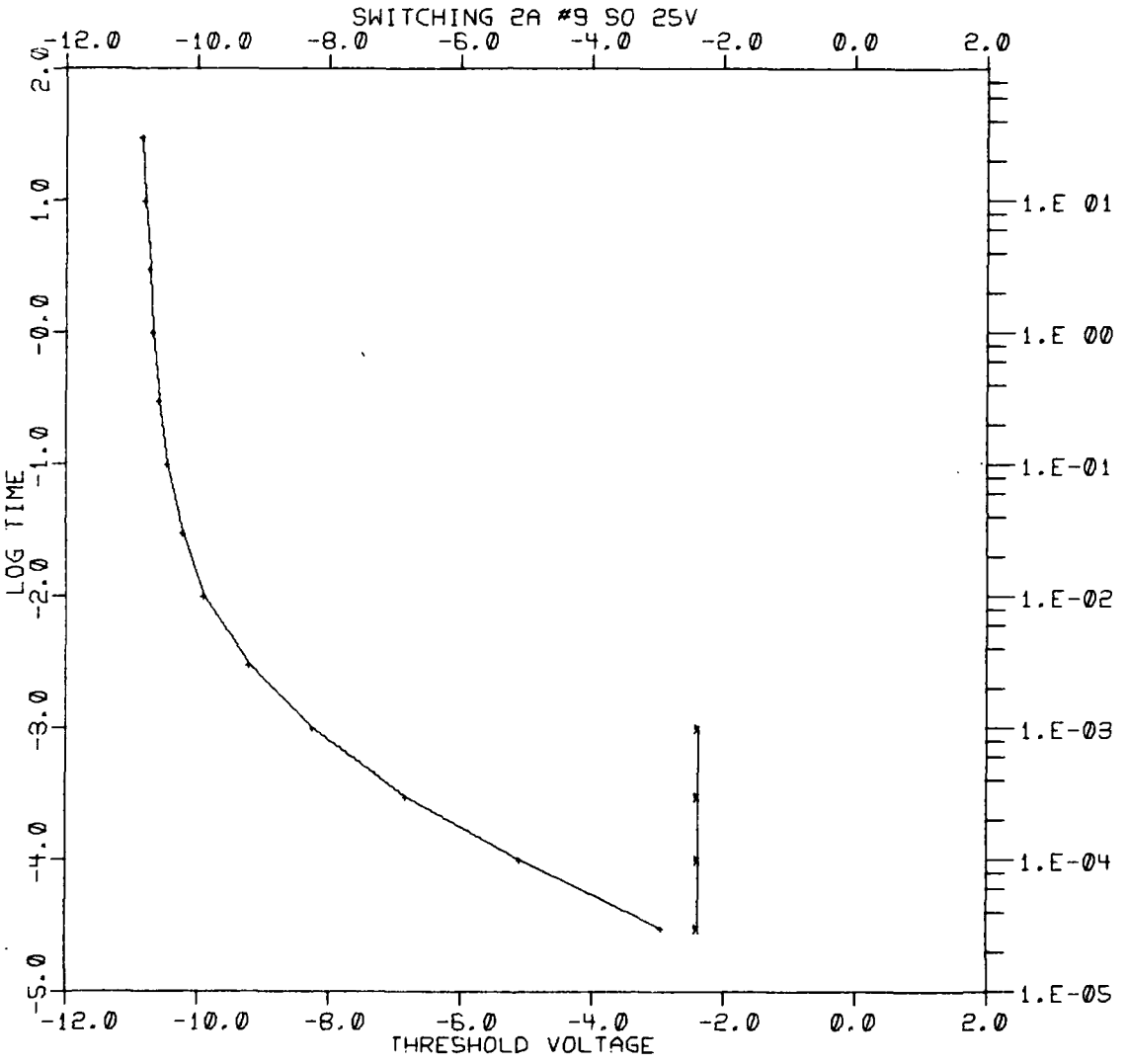

SWITCHING 2A #9 SO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-37

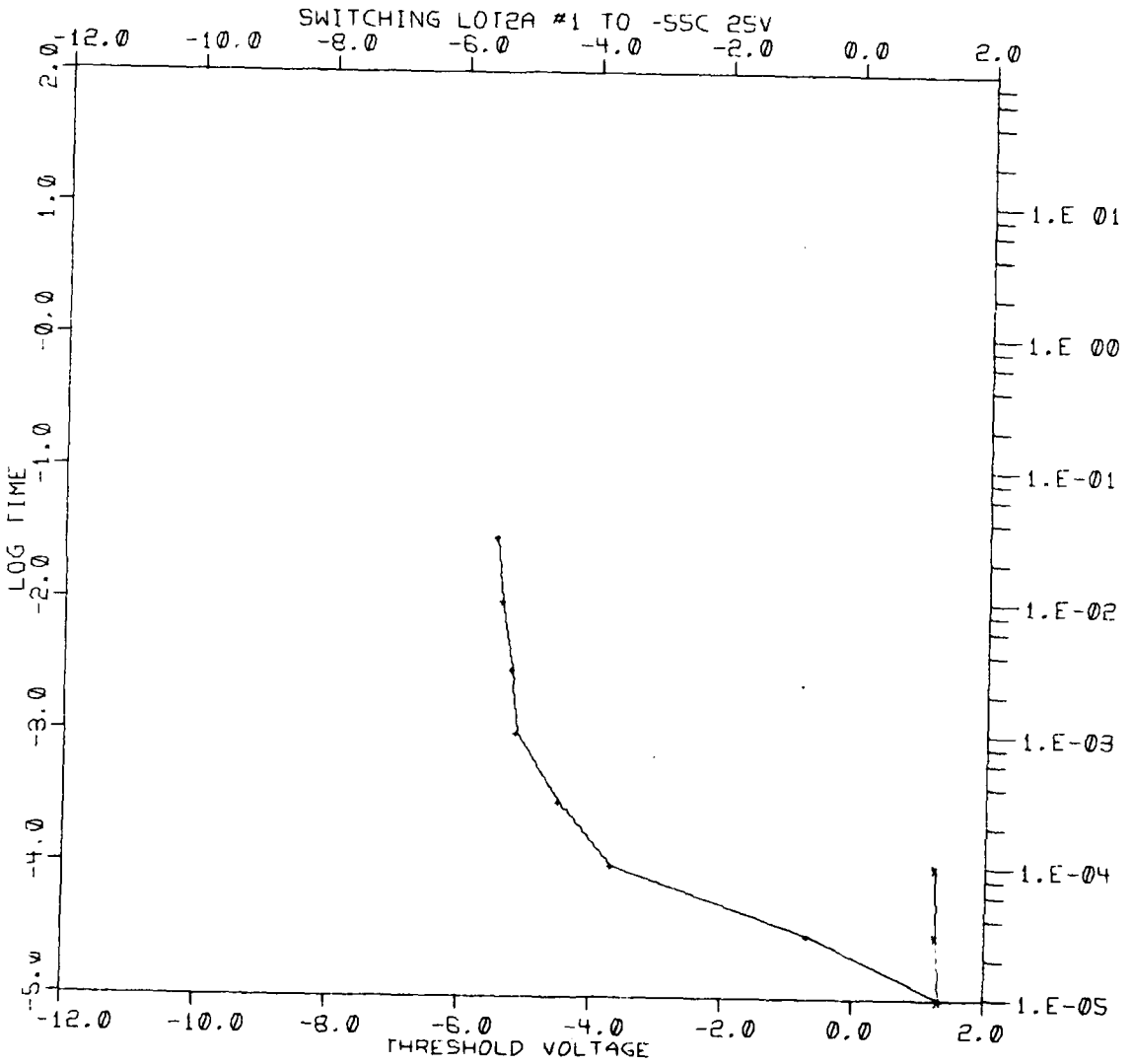

SWITCHING LOT2A #1 TO -55C 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-38

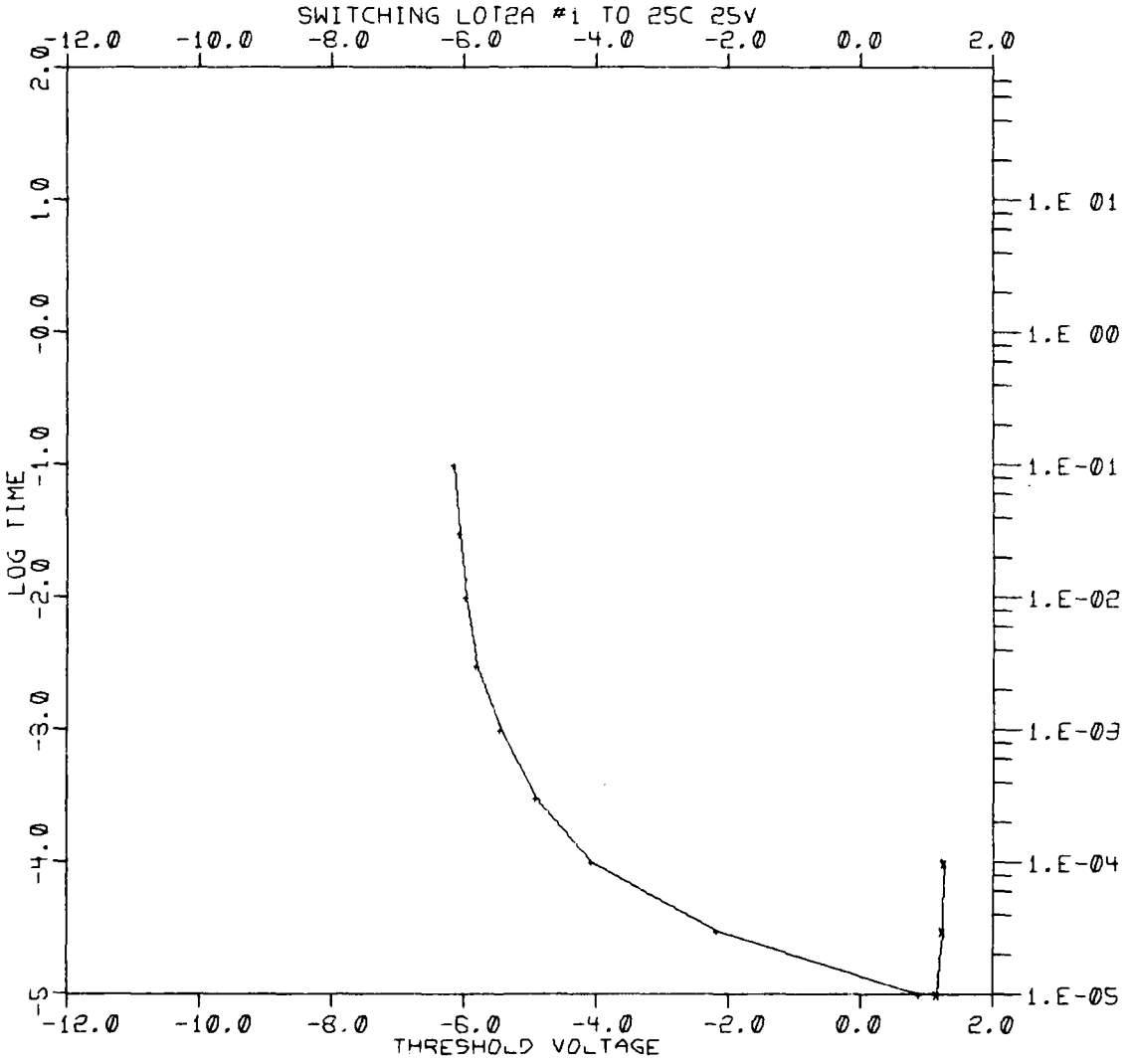

SWITCHING LOT2A #1 TO 25C 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-39

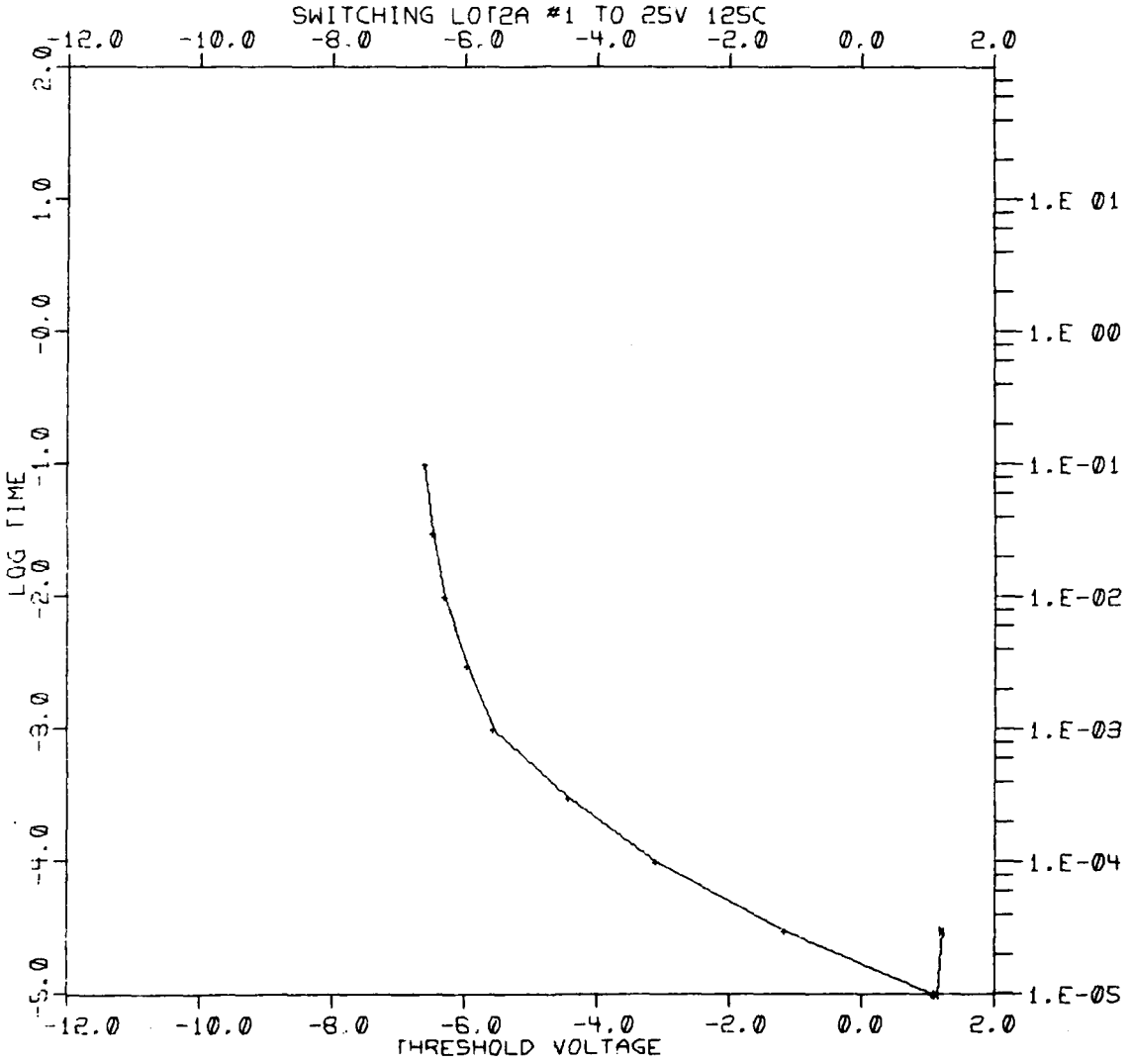

SWITCHING LOT2A #1 TO 25V 125C
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-40

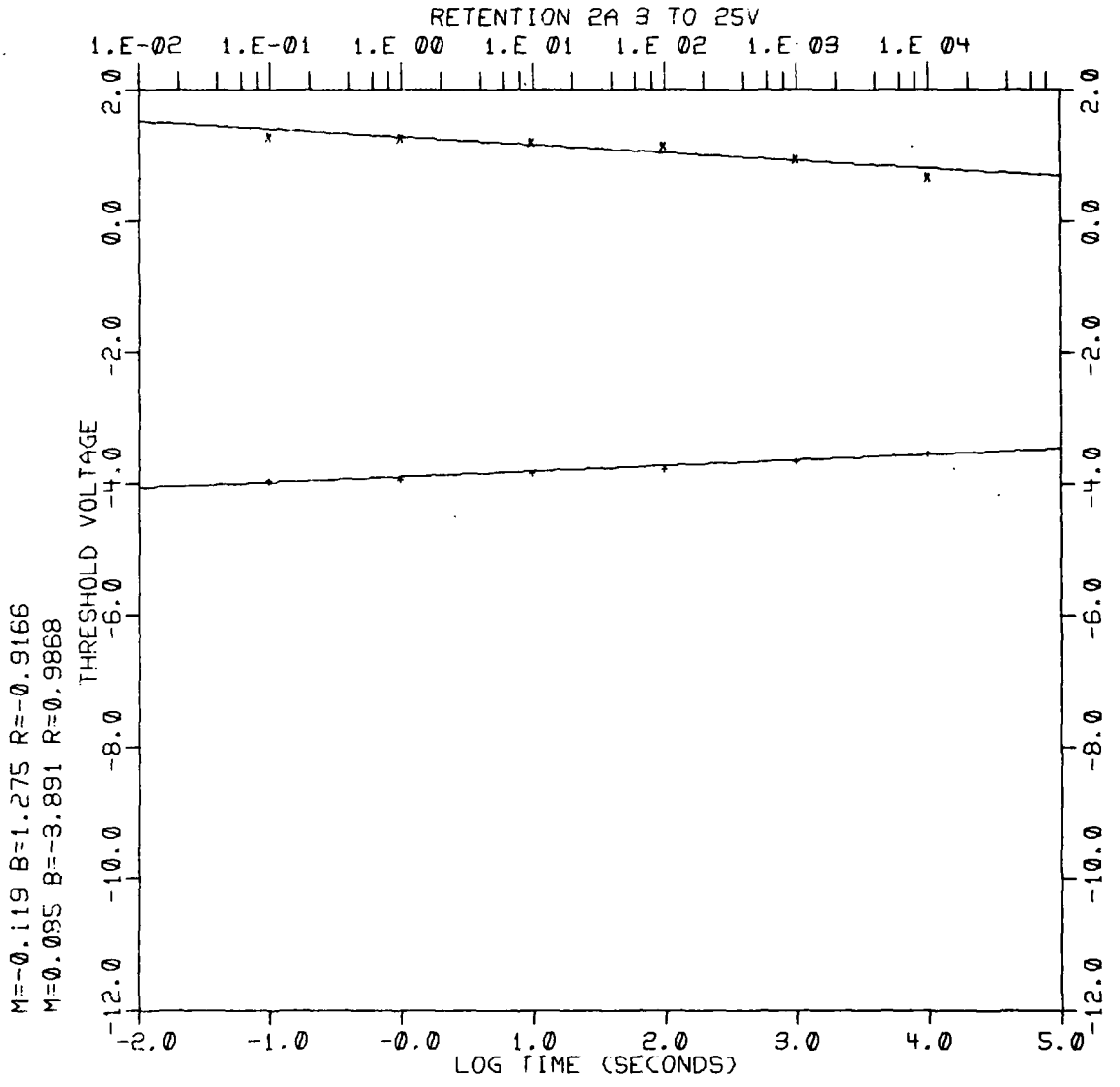

RETENTION 2A 3 TO 25V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
M=-0.119 B=1.275 R=-0.9166
M=0.095 B=-3.891 R=0.9868
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)

Fig. IV-41

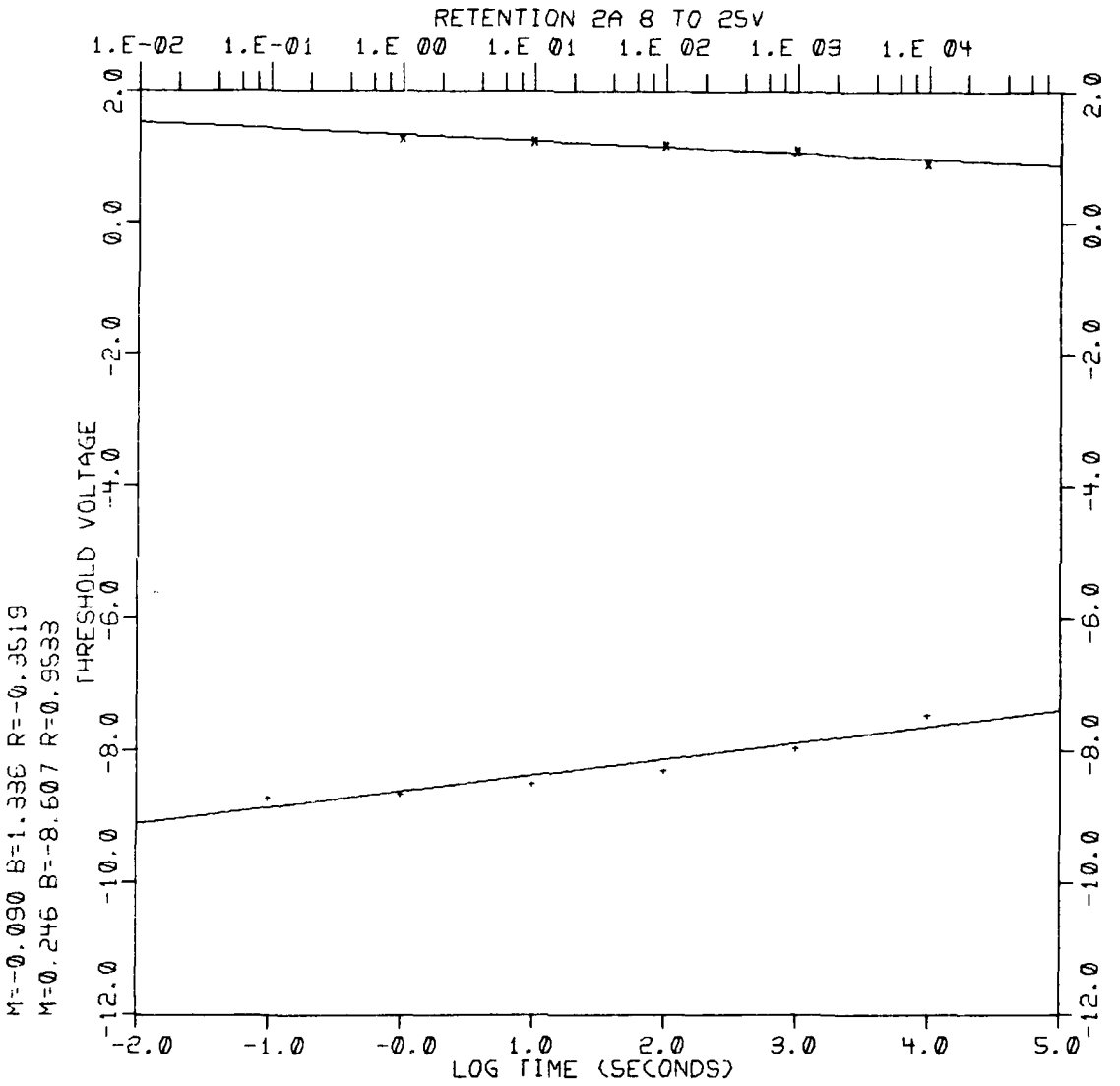
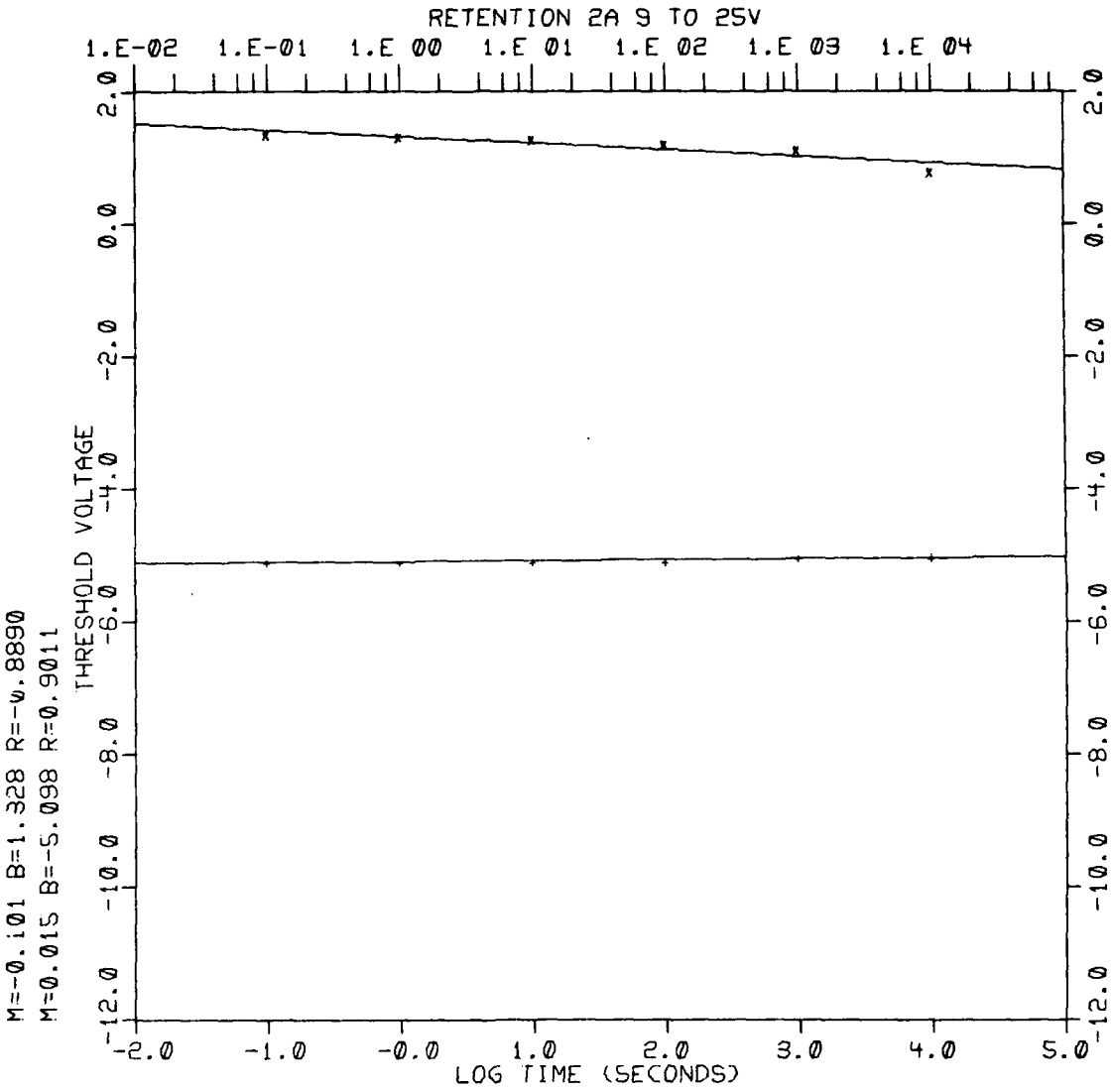
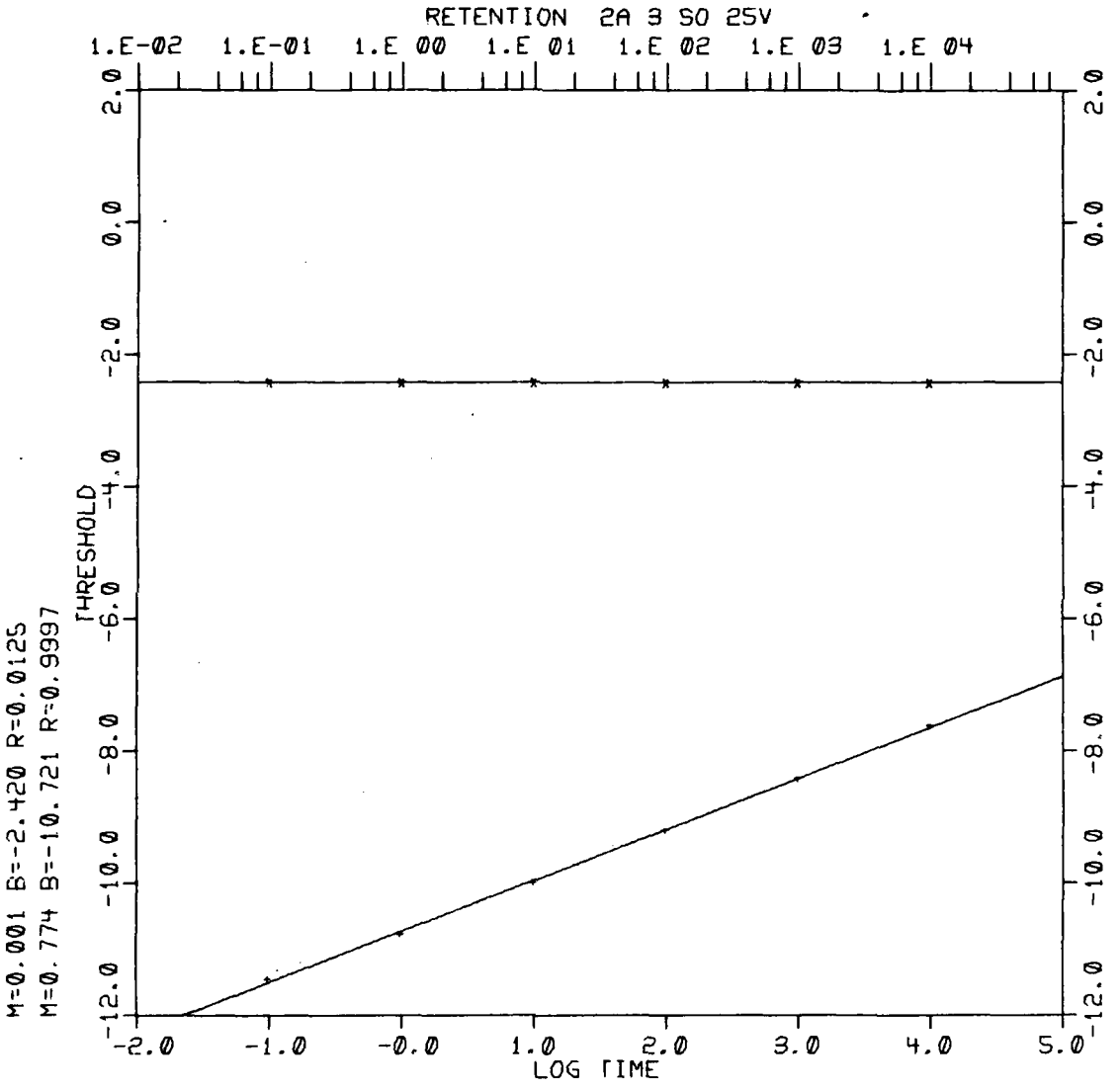

RETENTION 2A 8 TO 25V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
THRESHOLD VOLTAGE
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
M=-0.090 B=1.336 R=-0.3519
M=0.246 B=-8.607 R=0.9533
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)

Fig. IV-42



THIN OXIDE

Fig. IV-43



STEPPED OXIDE

Fig. IV-44

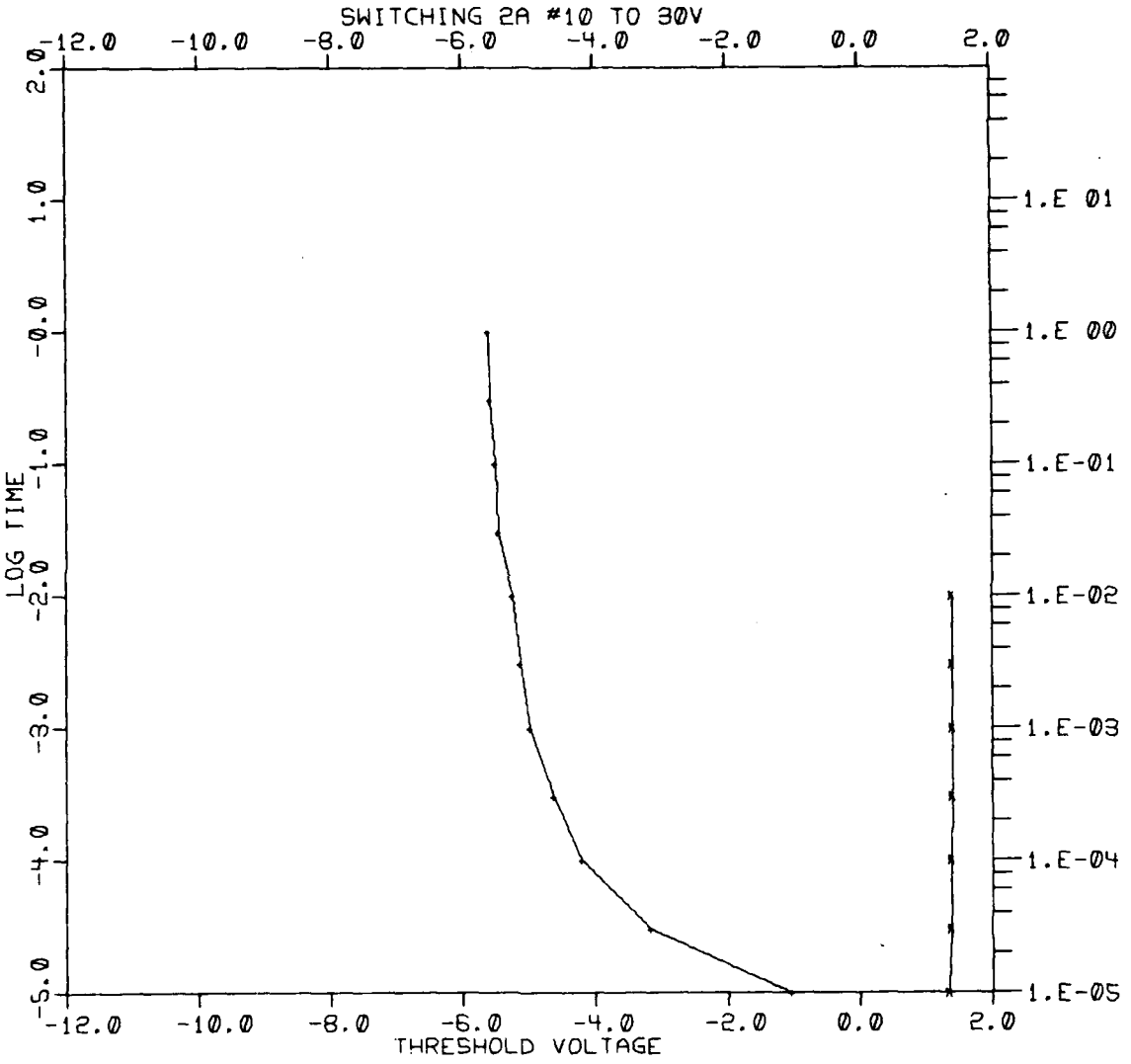

SWITCHING 2A #10 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-45

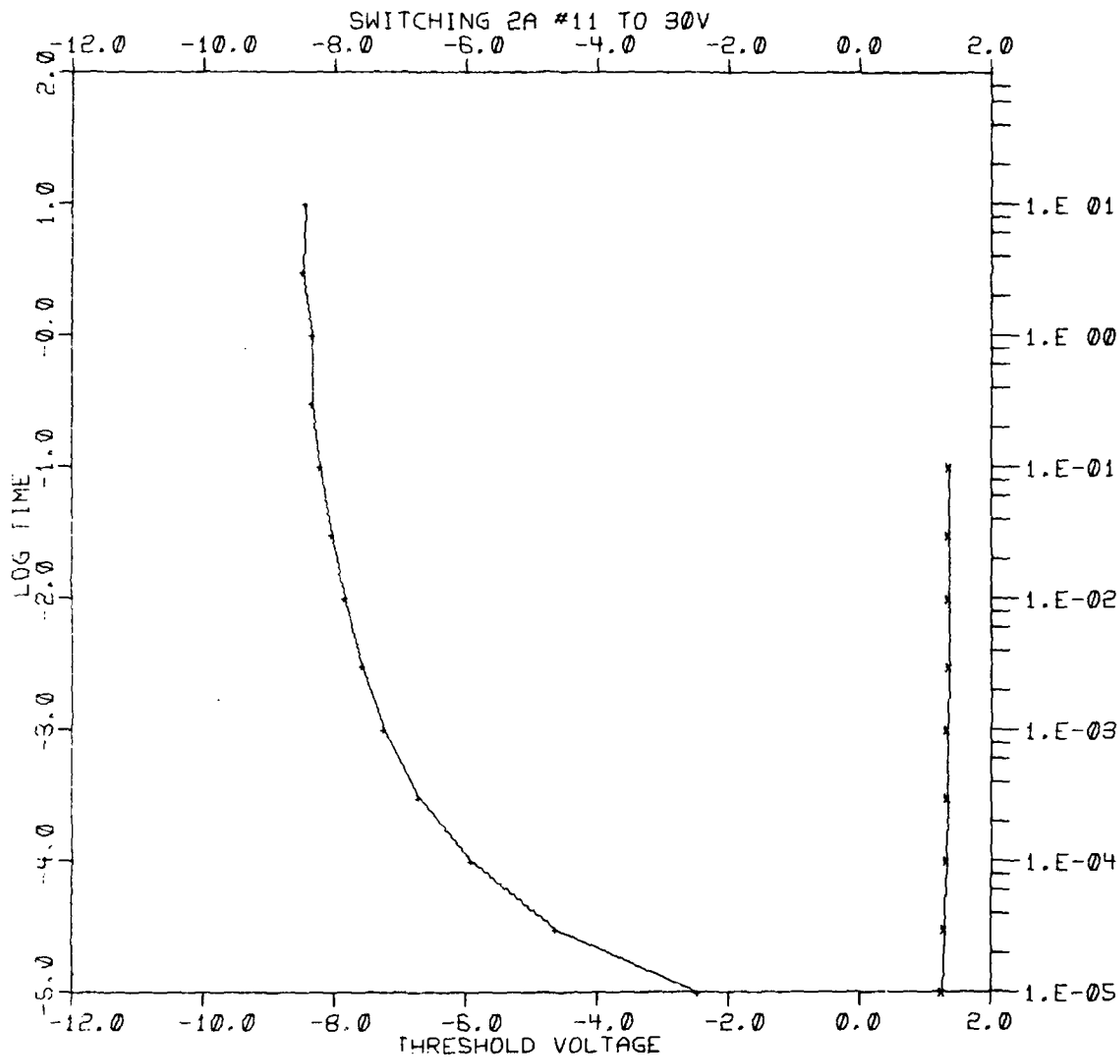

SWITCHING 2A #11 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-46

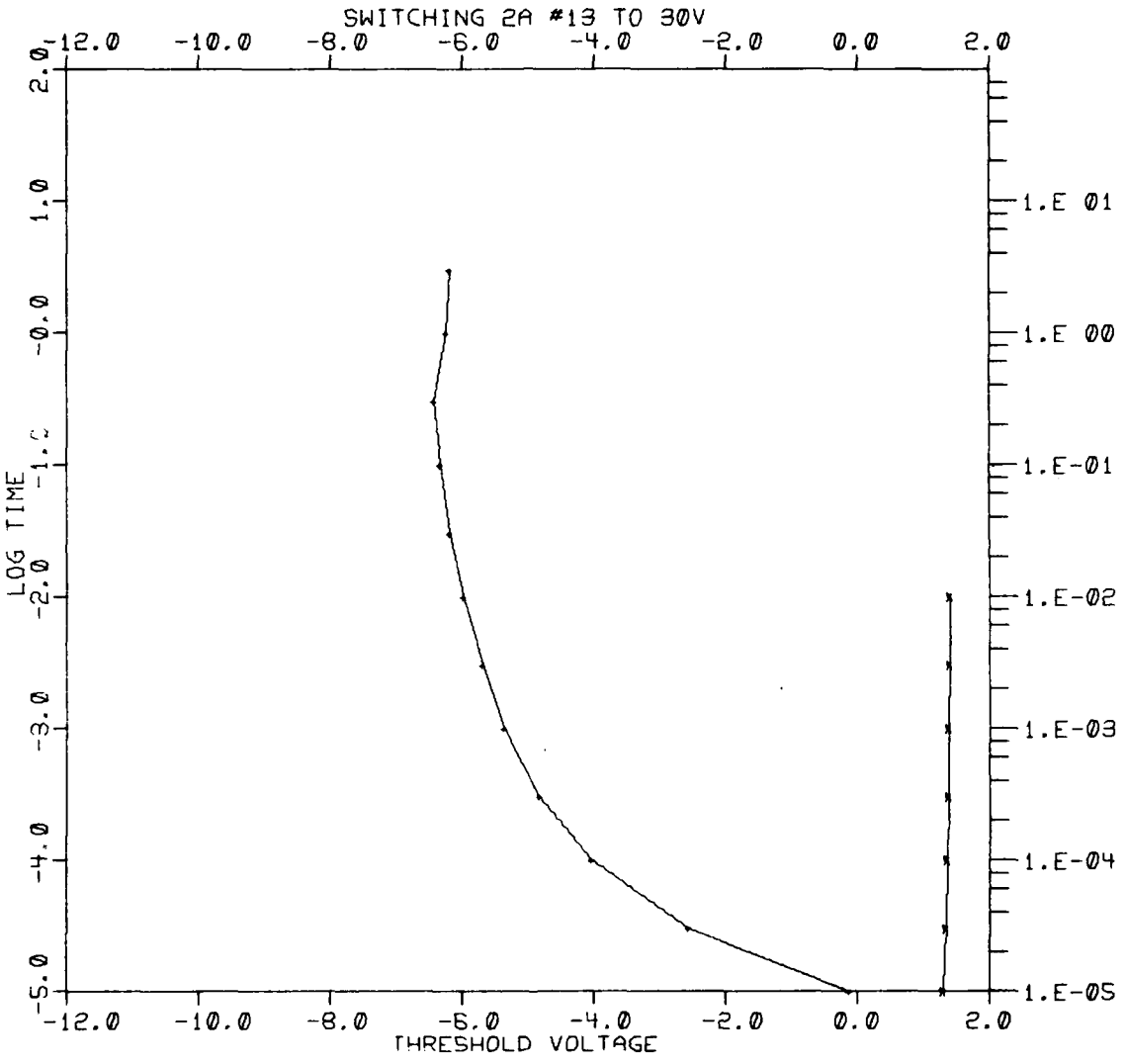

SWITCHING 2A #13 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-47

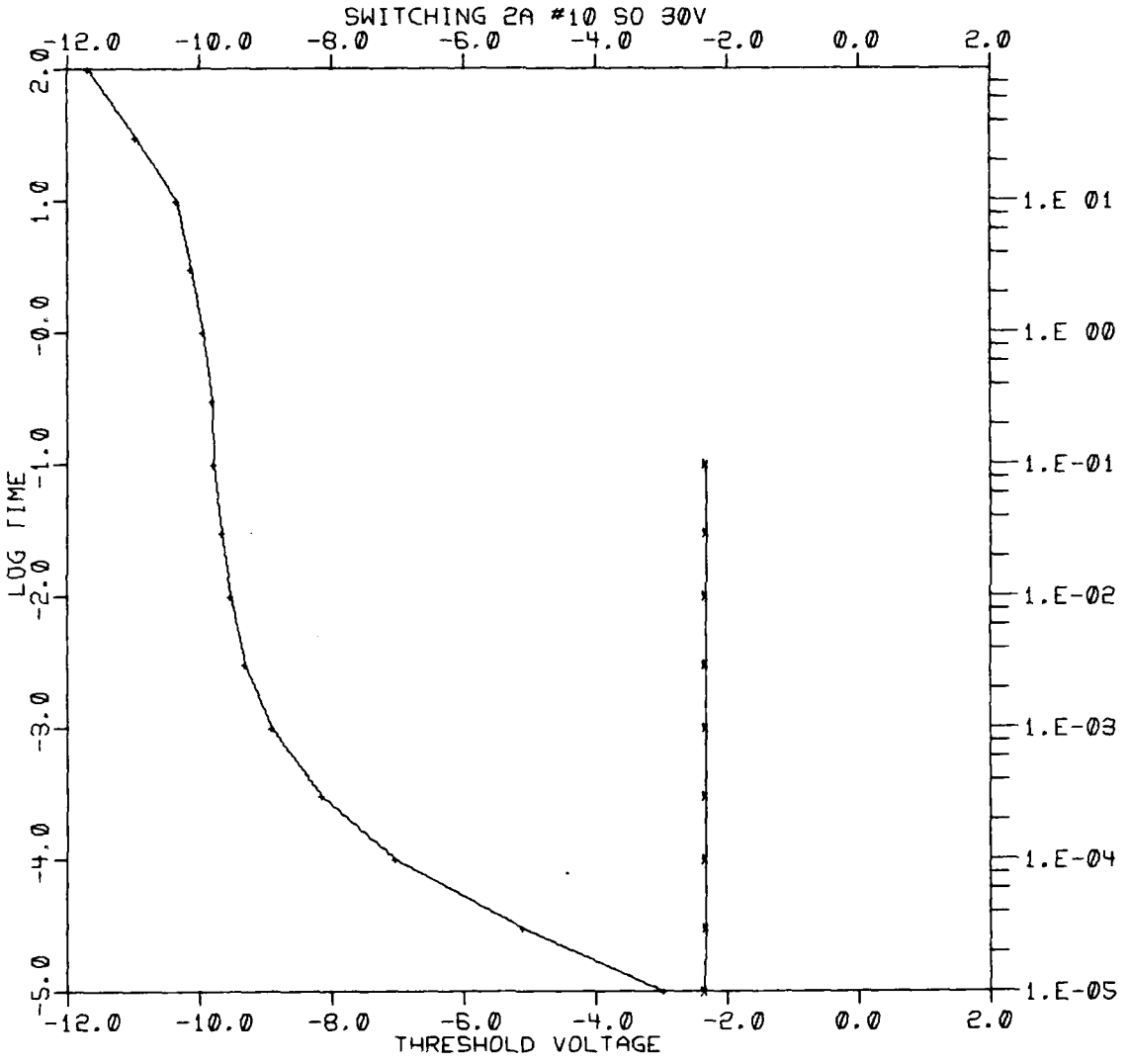

SWITCHING 2A #10 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-48

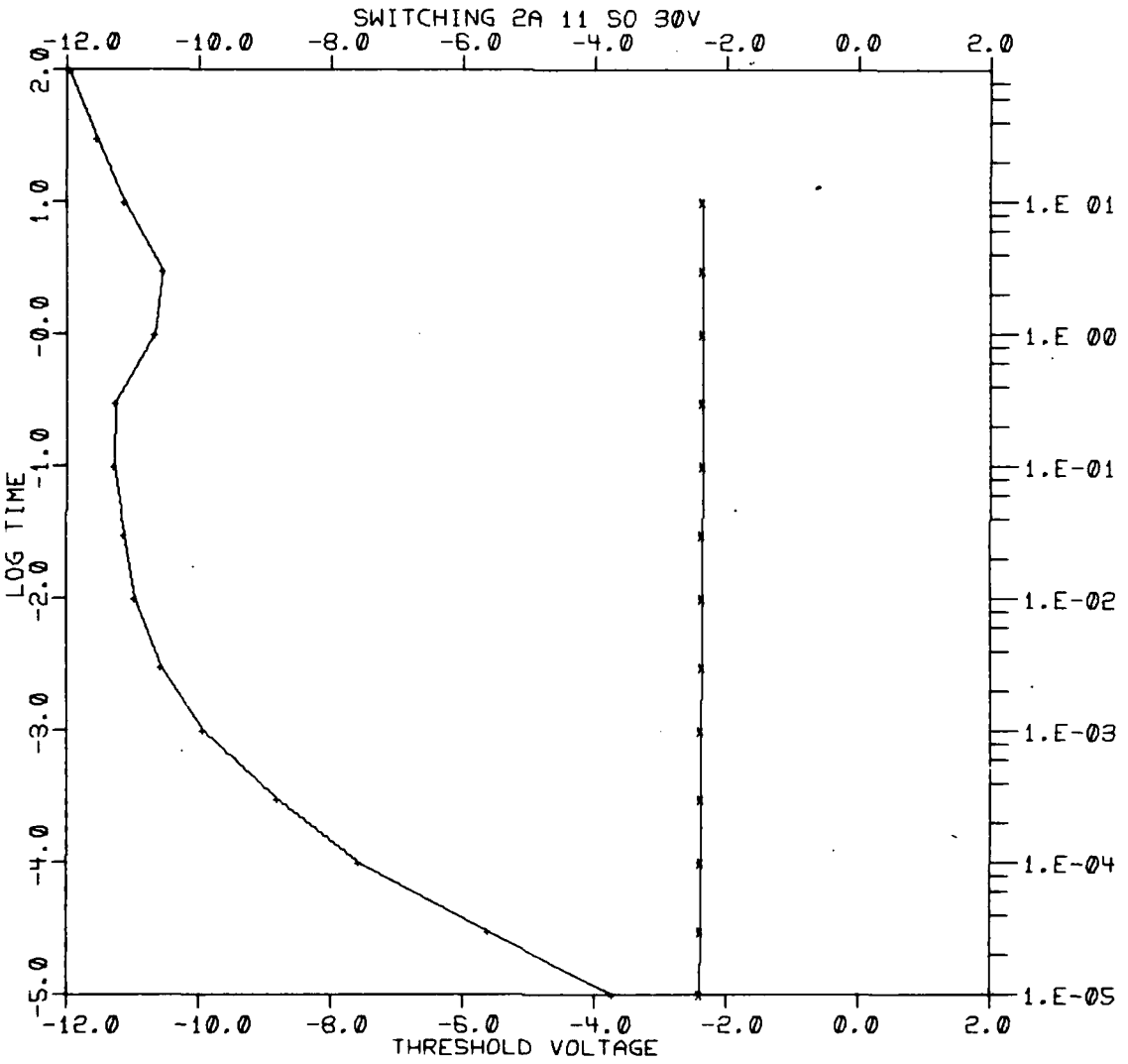
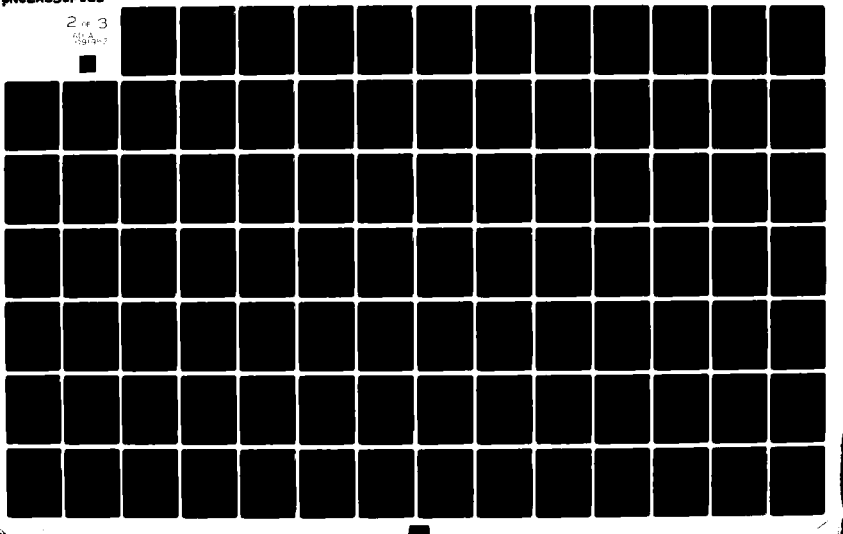

SWITCHING 2A 11 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-49

AD-A091 952 RCA SOLID STATE DIV SOMERVILLE NJ F/G 9/5
FEASIBILITY STUDY OF THE COMBINATION OF MNOS ELEMENTS AND BIPOL--ETC(U)
AUG 80 K CUNNIFF F19628-78-C-0178
UNCLASSIFIED RADC-TR-80-177 NL

2 OF 3
AD A091952



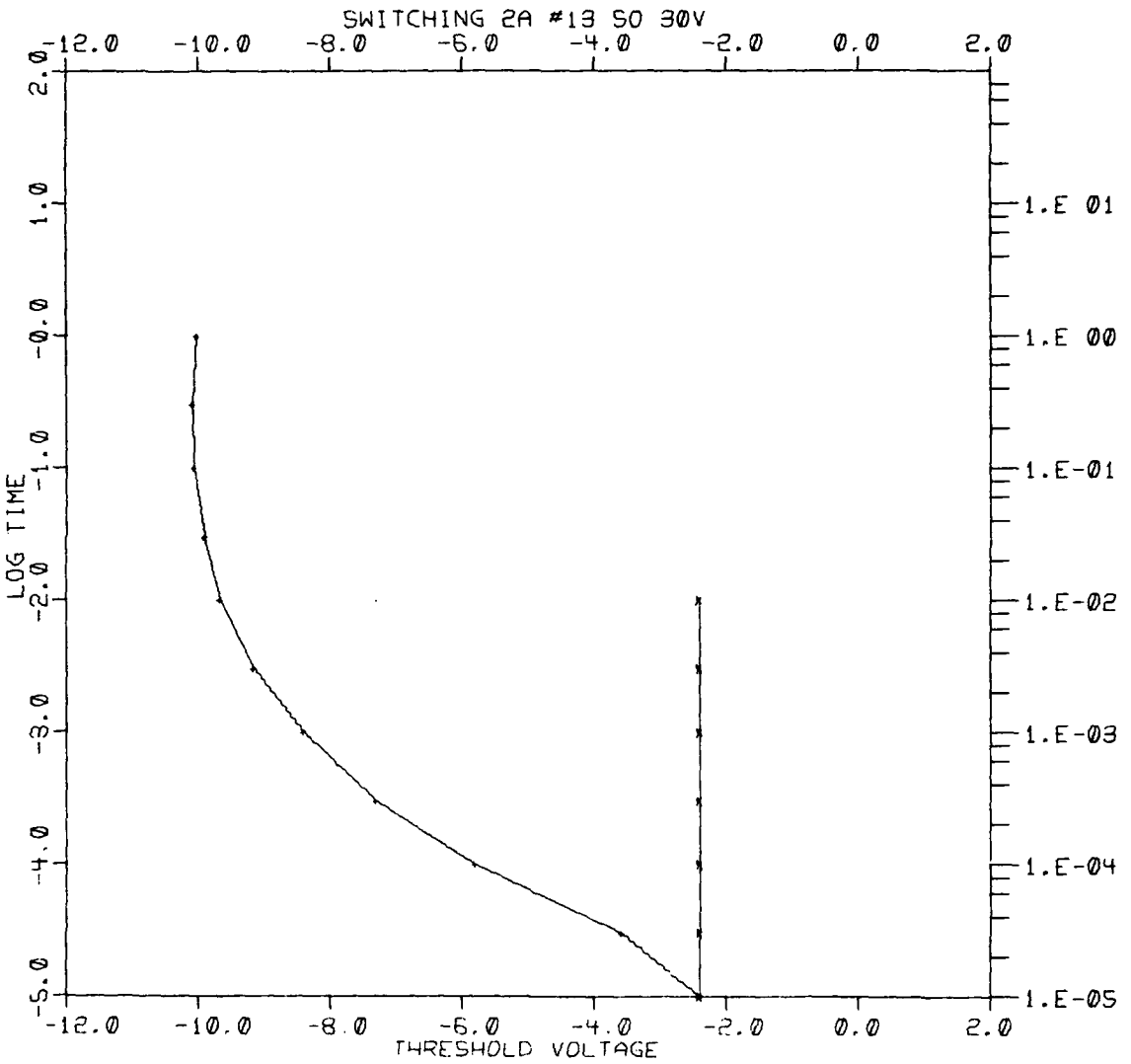

SWITCHING 2A #13 50 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-50

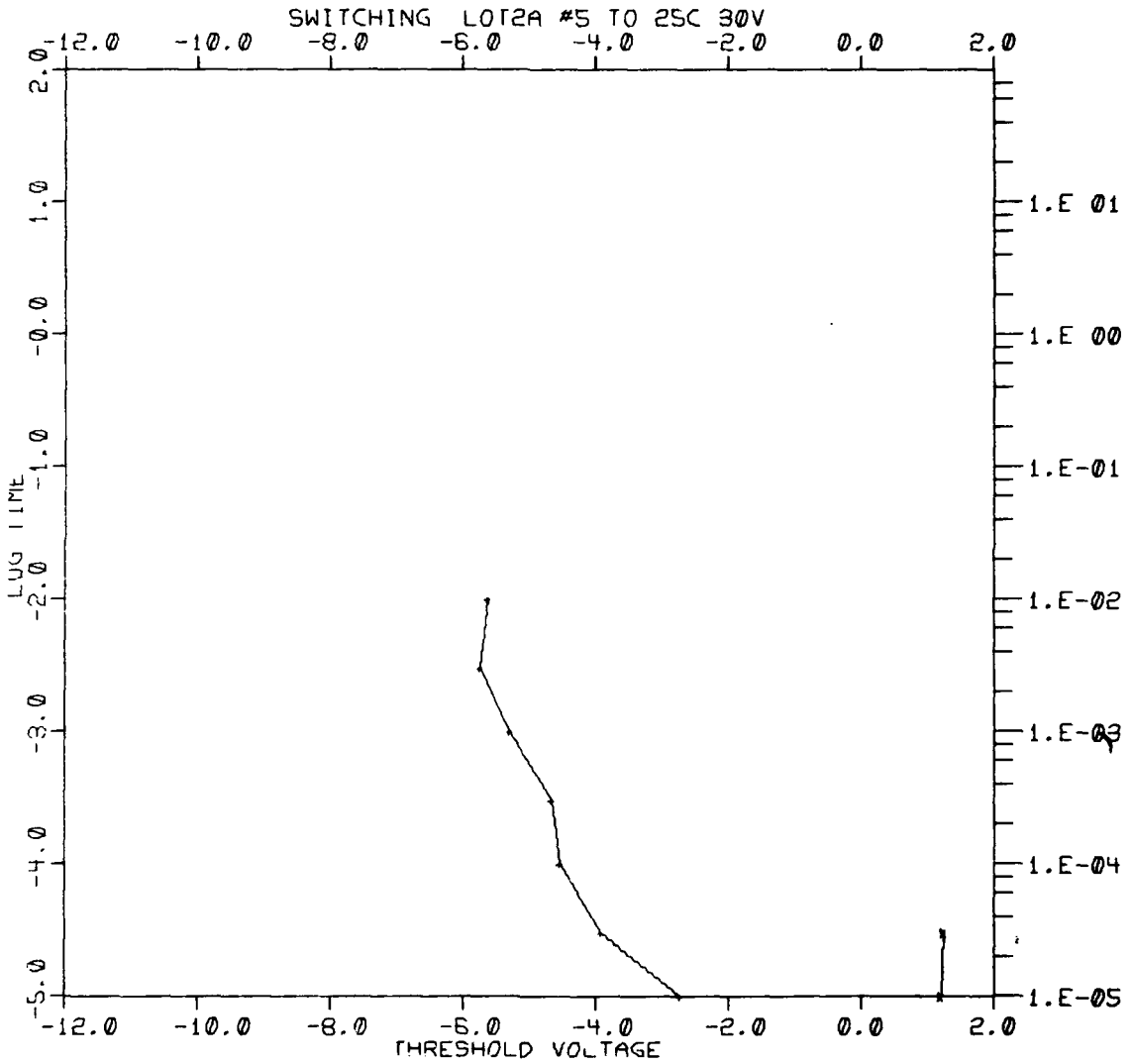

SWITCHING LOT2A #5 TO 25C 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG I IMI
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-51

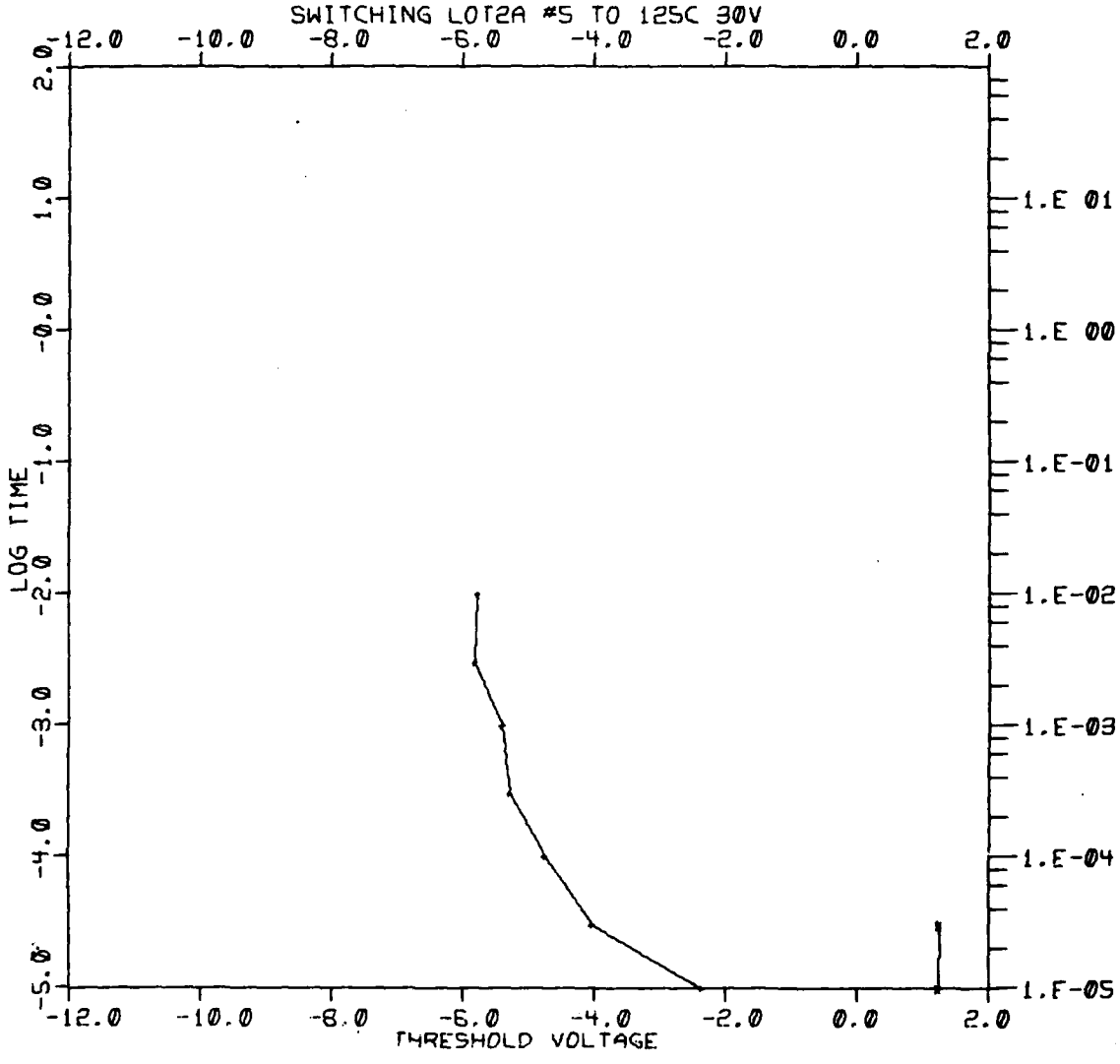

SWITCHING LOT2A #5 TO 125C 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
LOG TIME
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-52

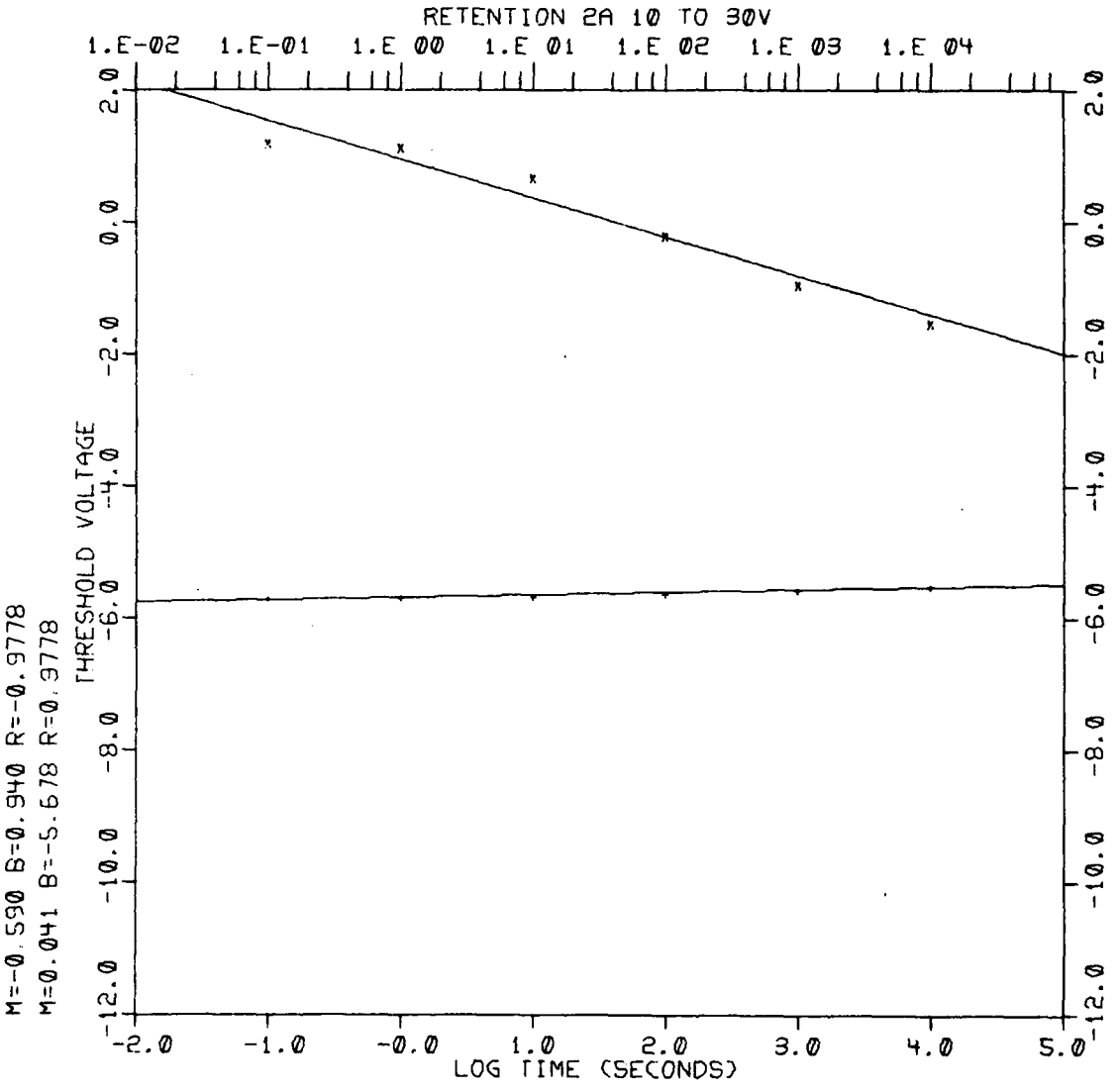

RETENTION 2A 10 TO 30V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
M=-0.590 B=0.940 R=-0.9778
M=0.041 B=-5.678 R=0.9778
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)

Fig. IV-53

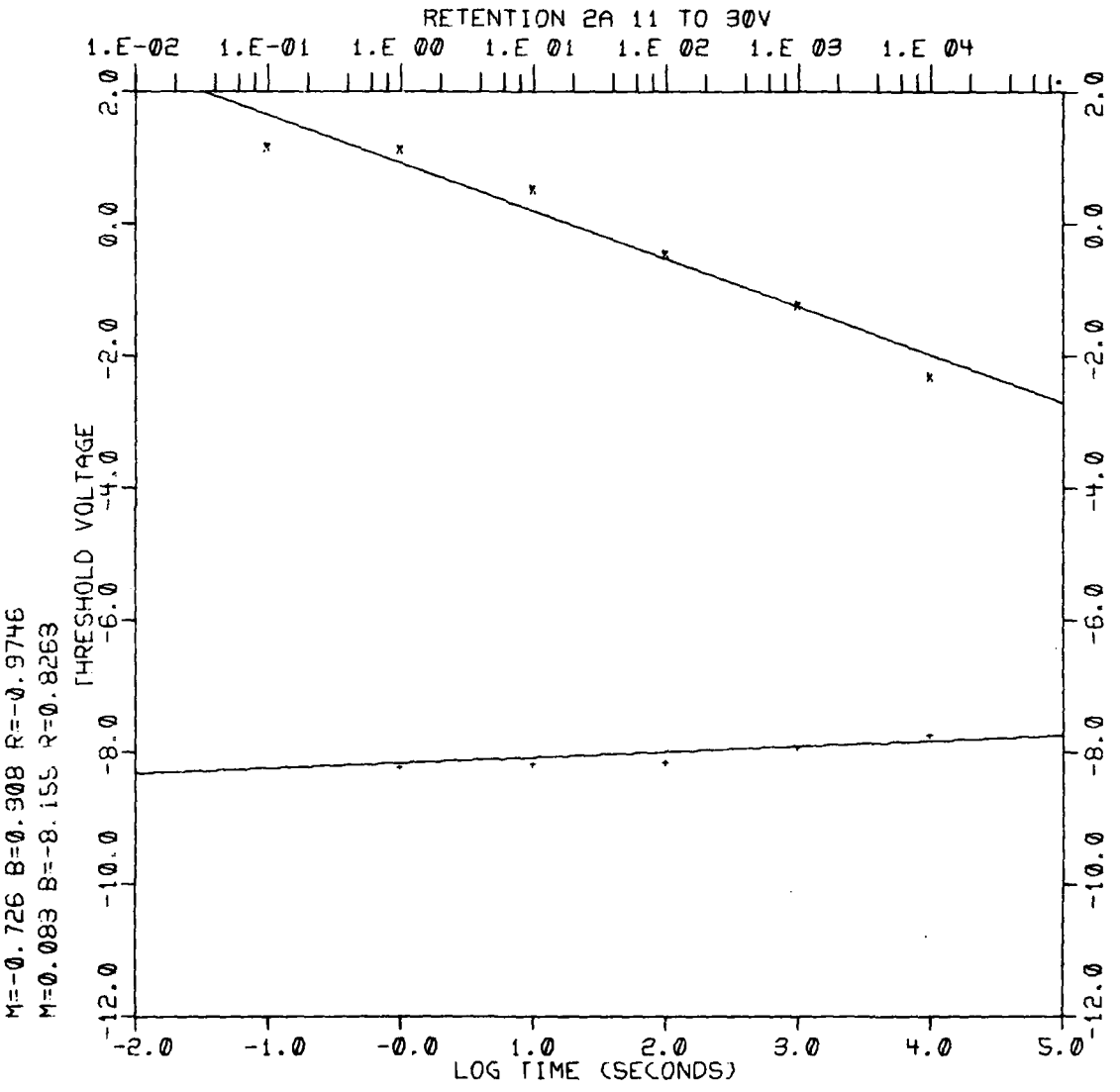

RETENTION 2A 11 TO 30V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
M=-0.726 B=0.308 R=-0.9746
M=0.083 B=-8.155 R=0.8263
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)

Fig. IV-54

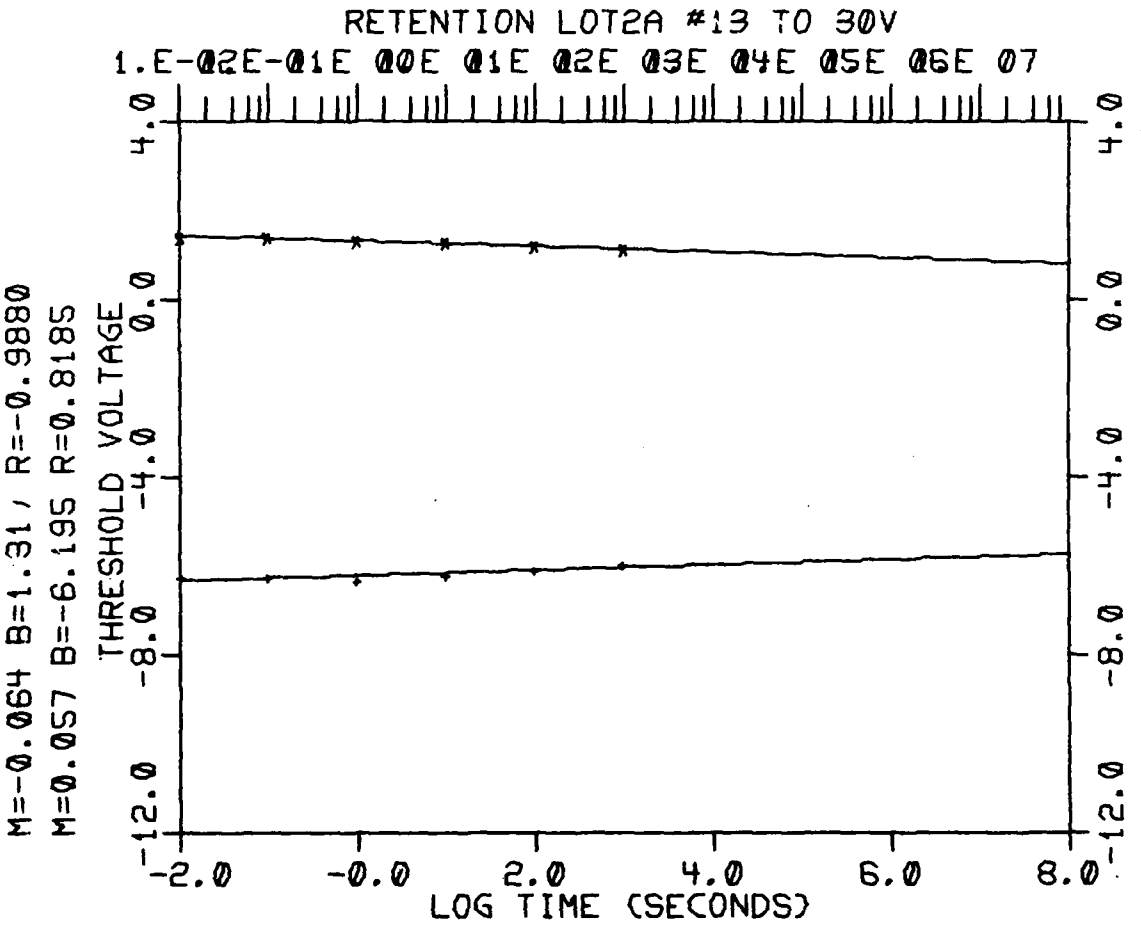

RETENTION LOT2A #13 TO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.064 B=1.31 / R=-0.9880
M=0.057 B=-6.195 R=0.8185
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-55

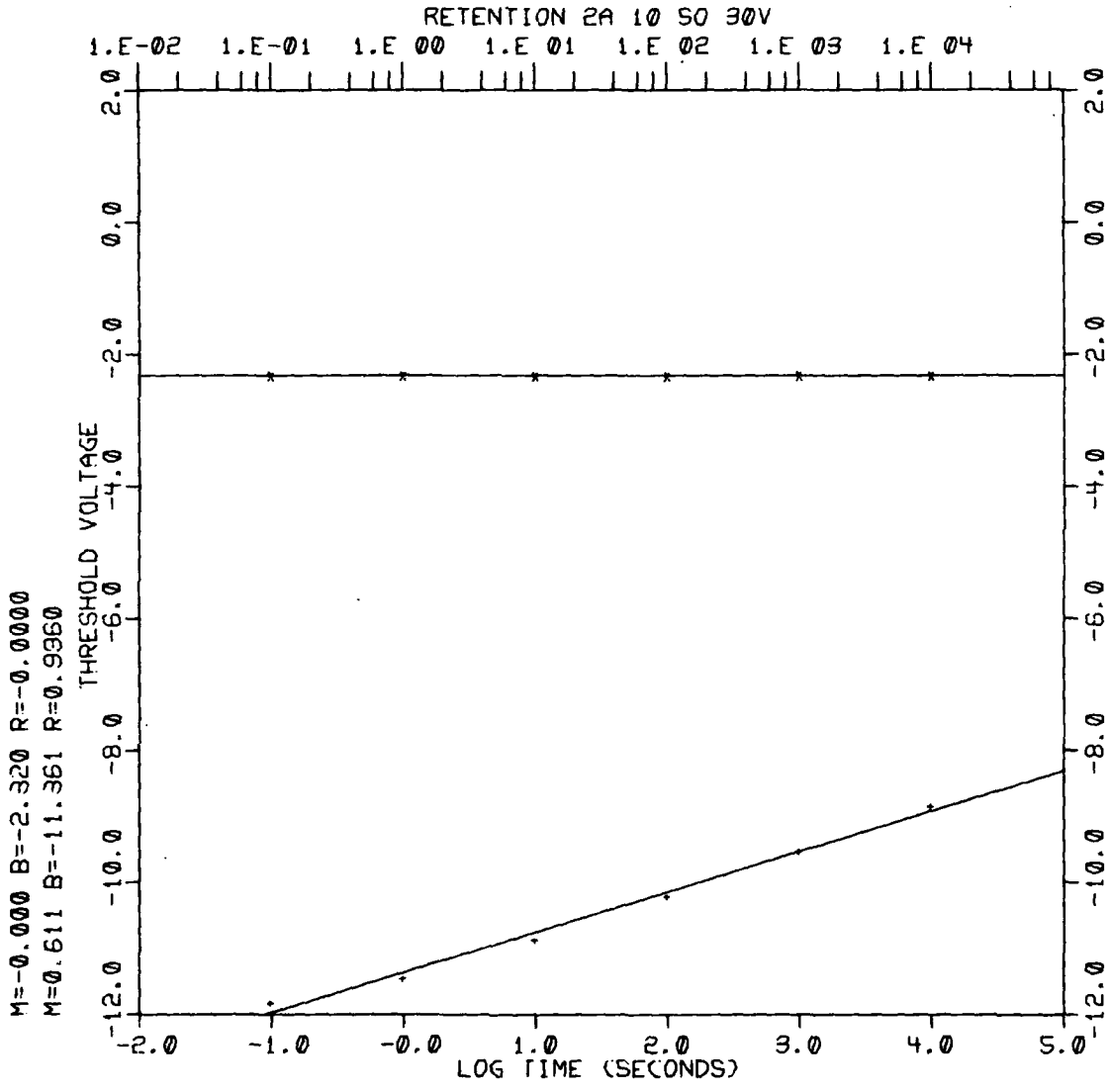

RETENTION 2A 10 SO 30V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
M=-0.000 B=-2.320 R=-0.0000
M=0.611 B=-11.361 R=0.9960
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)

Fig. IV-56

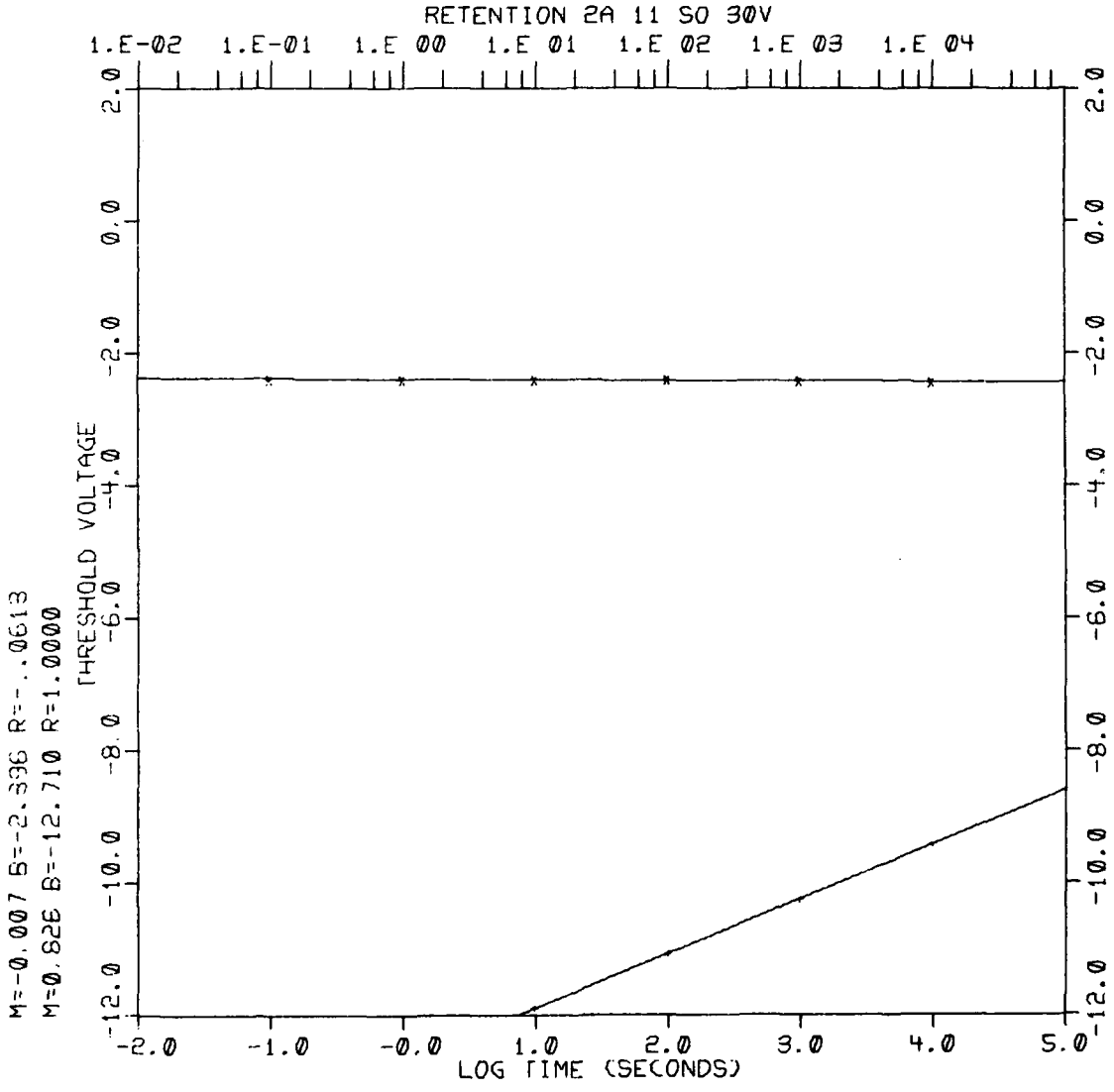

RETENTION 2A 11 SO 30V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
M=-0.007 B=-2.396 R=-.0613
M=0.826 B=-12.710 R=1.0000
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)

Fig. IV-57

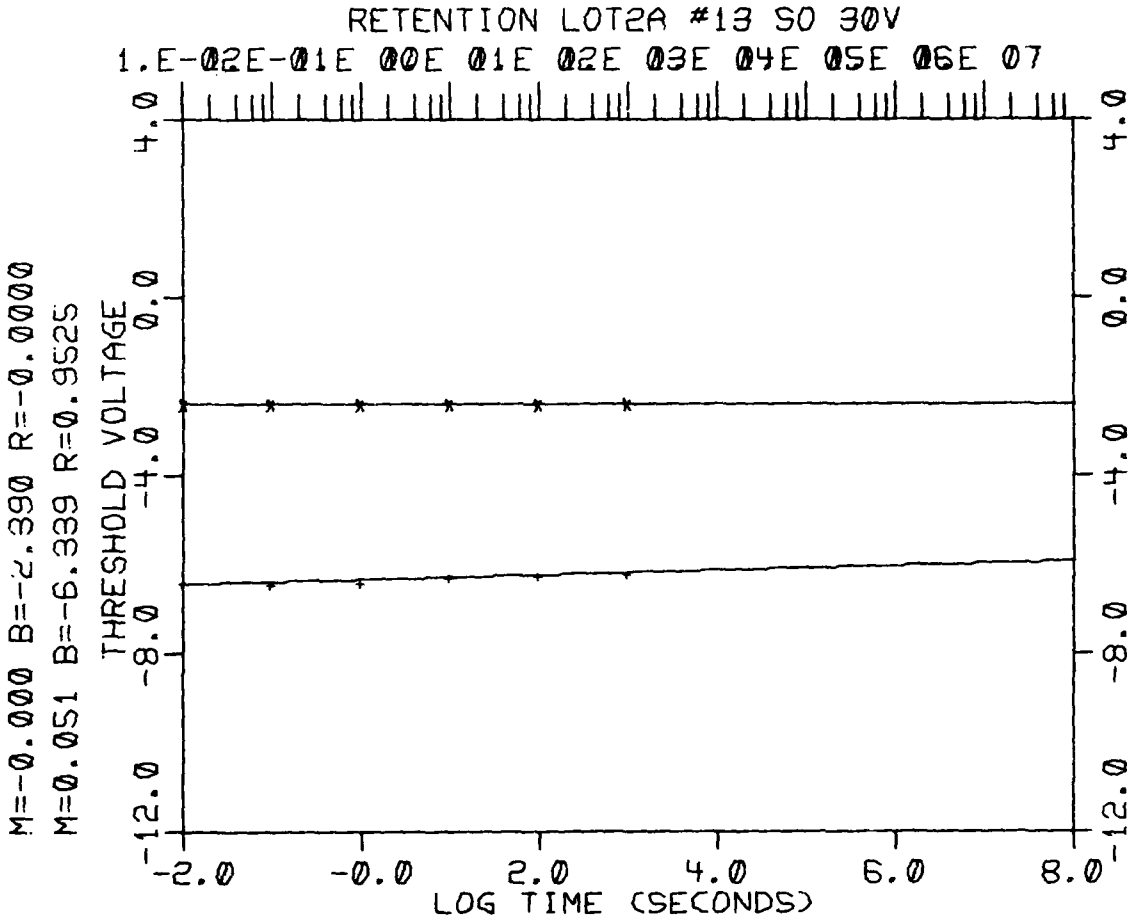

RETENTION LOT2A #13 SO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.390 R=-0.0000
M=0.051 B=-6.339 R=0.9525
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-58

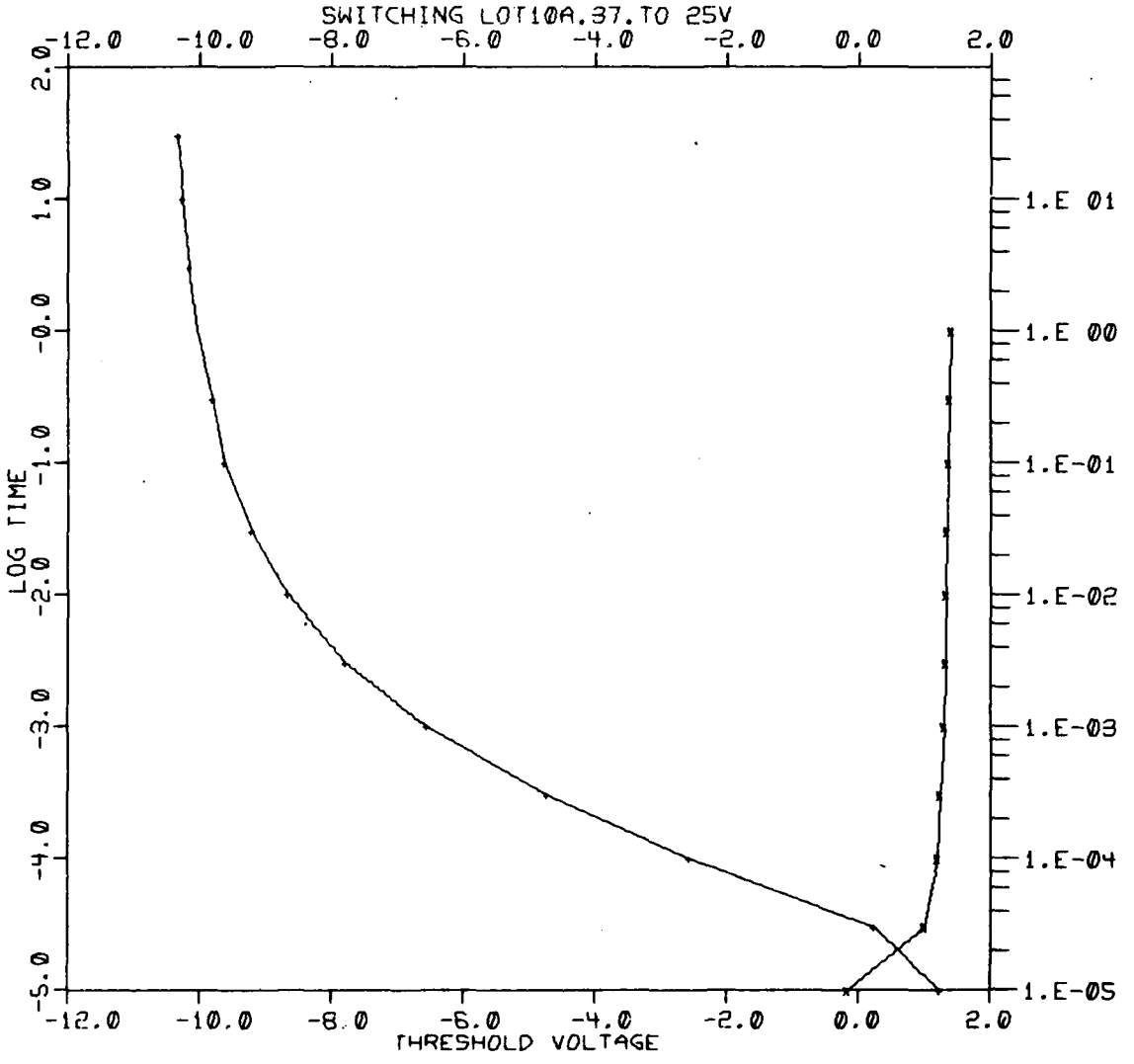

SWITCHING LOT10A.37.TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-59

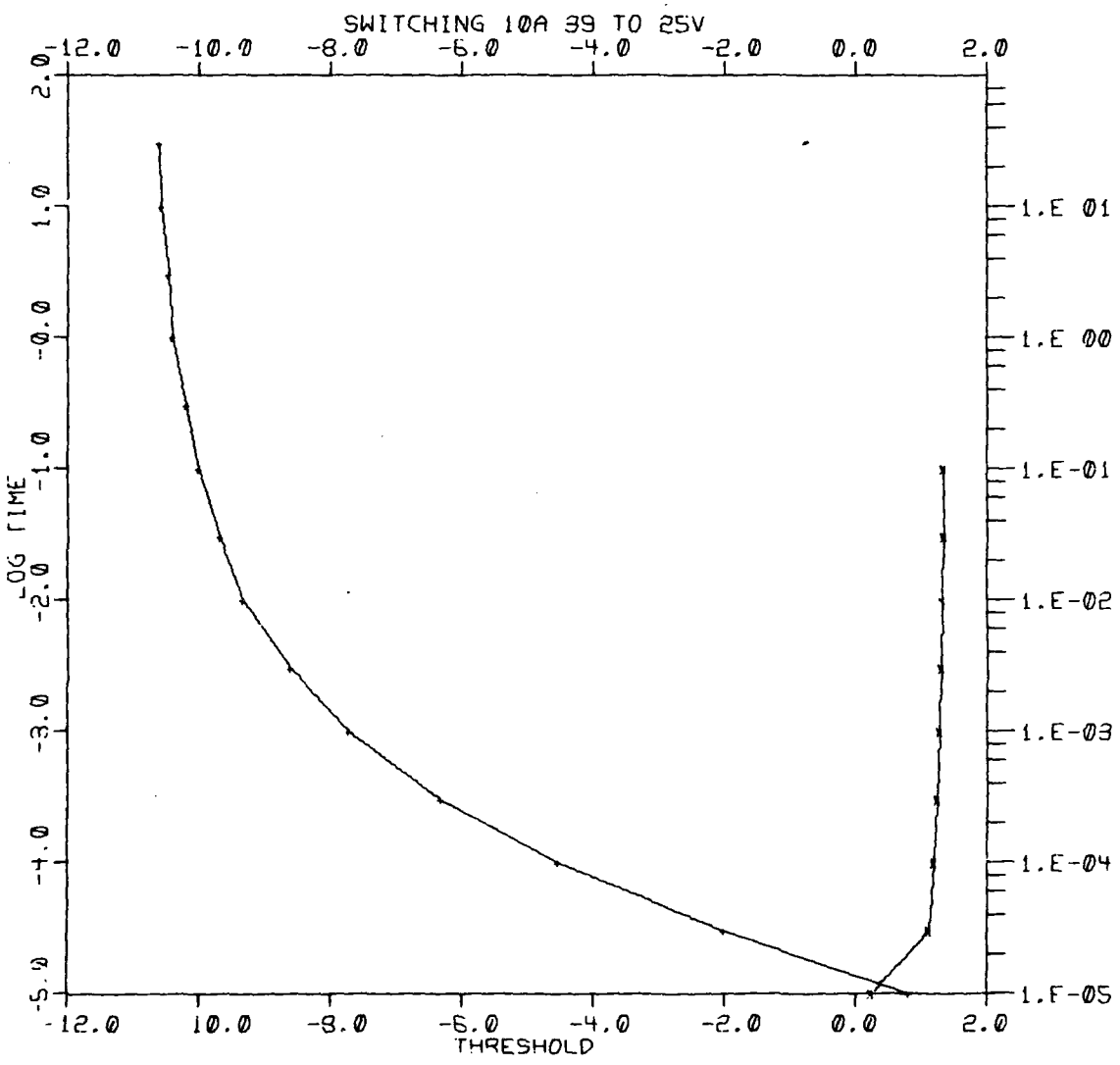

SWITCHING 10A 39 TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
-12.0
10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
THRESHOLD

Fig. IV-60

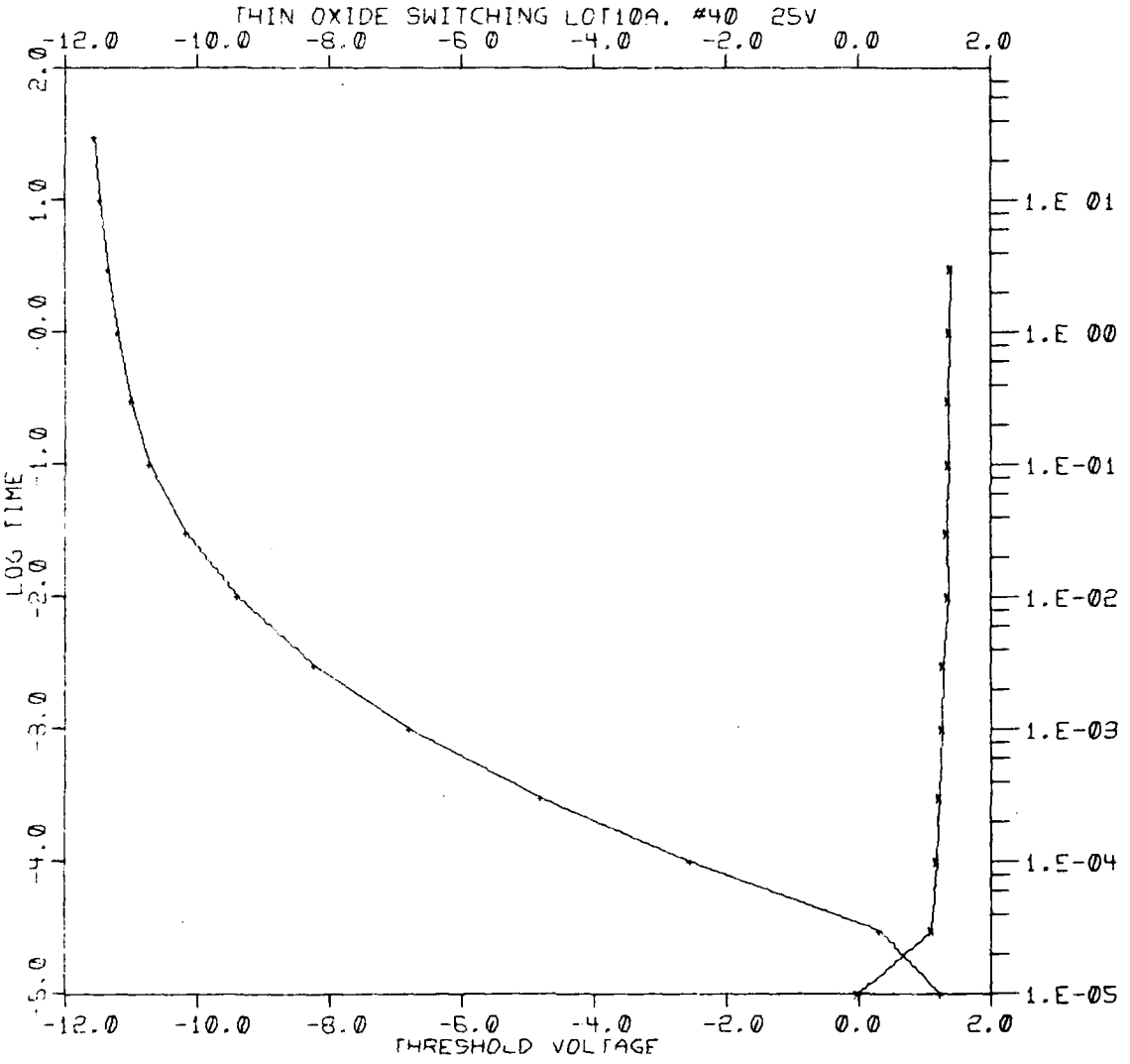

THIN OXIDE SWITCHING LOT10A. #40 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-61

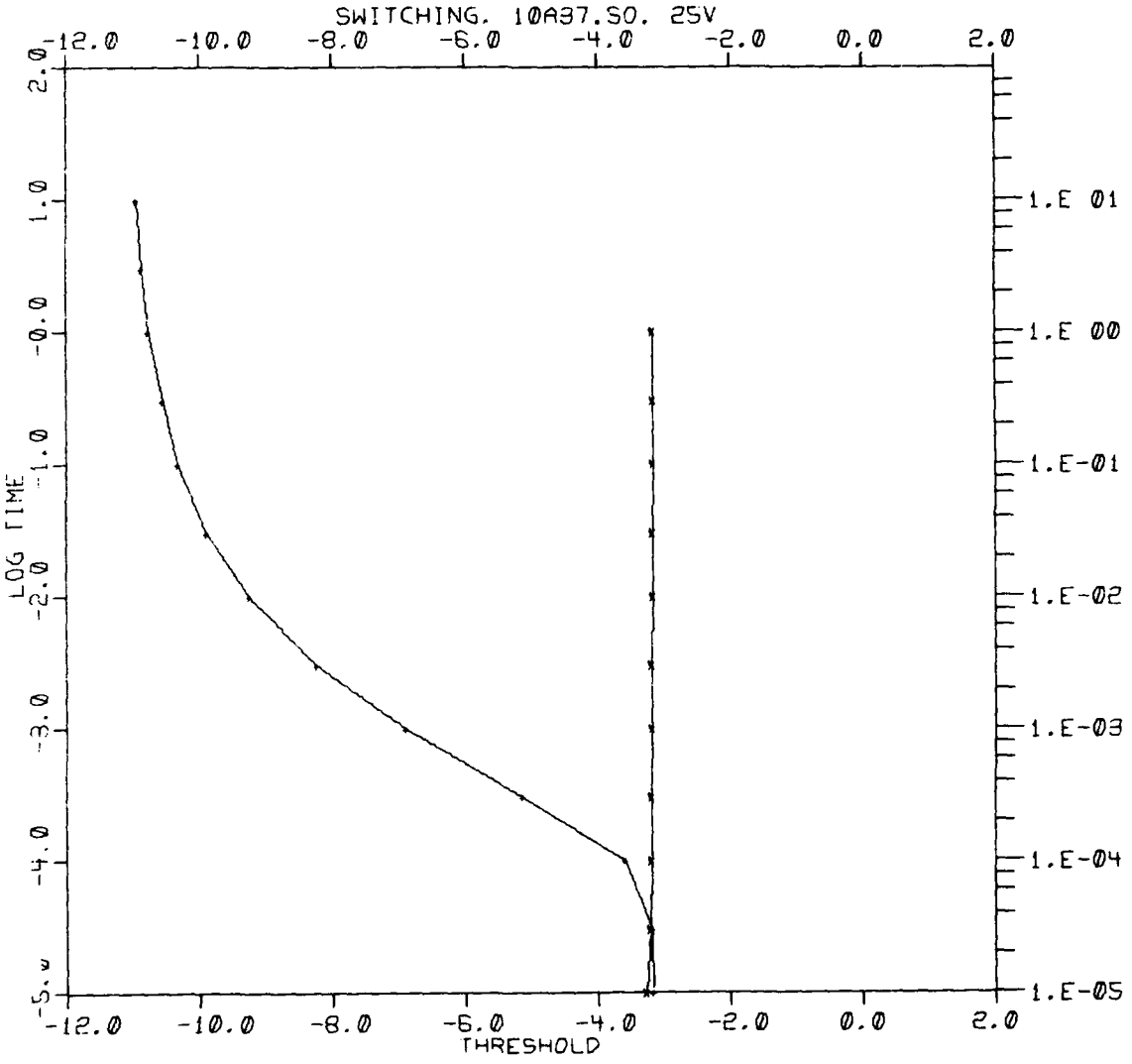

SWITCHING. 10A37.SO. 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
LOG TIME
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-62

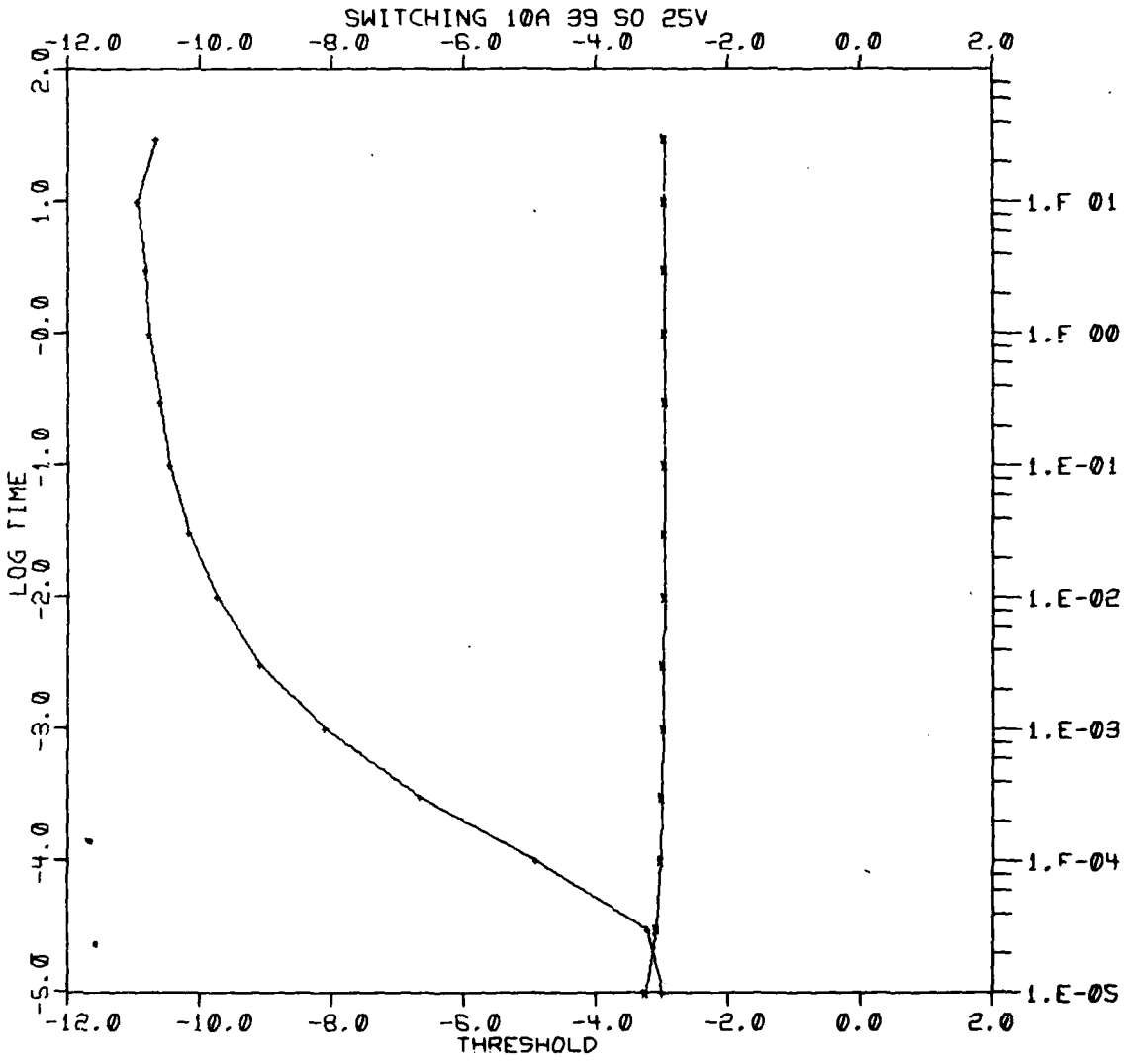

SWITCHING 10A 39 SO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.F 01
1.F 00
1.E-01
1.E-02
1.E-03
1.F-04
1.E-05
THRESHOLD

Fig. IV-63

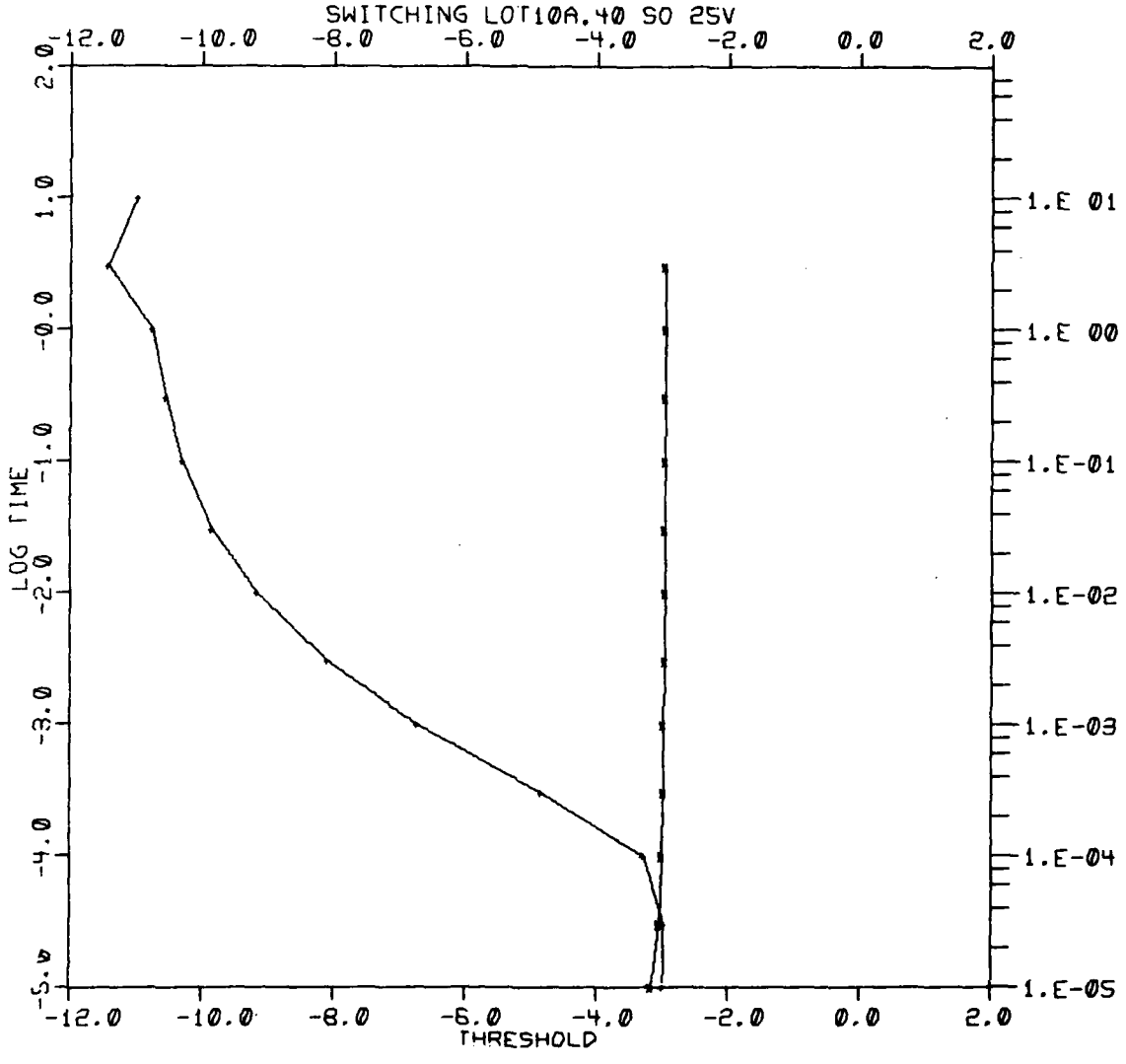

SWITCHING LOT10A.40 SO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-64

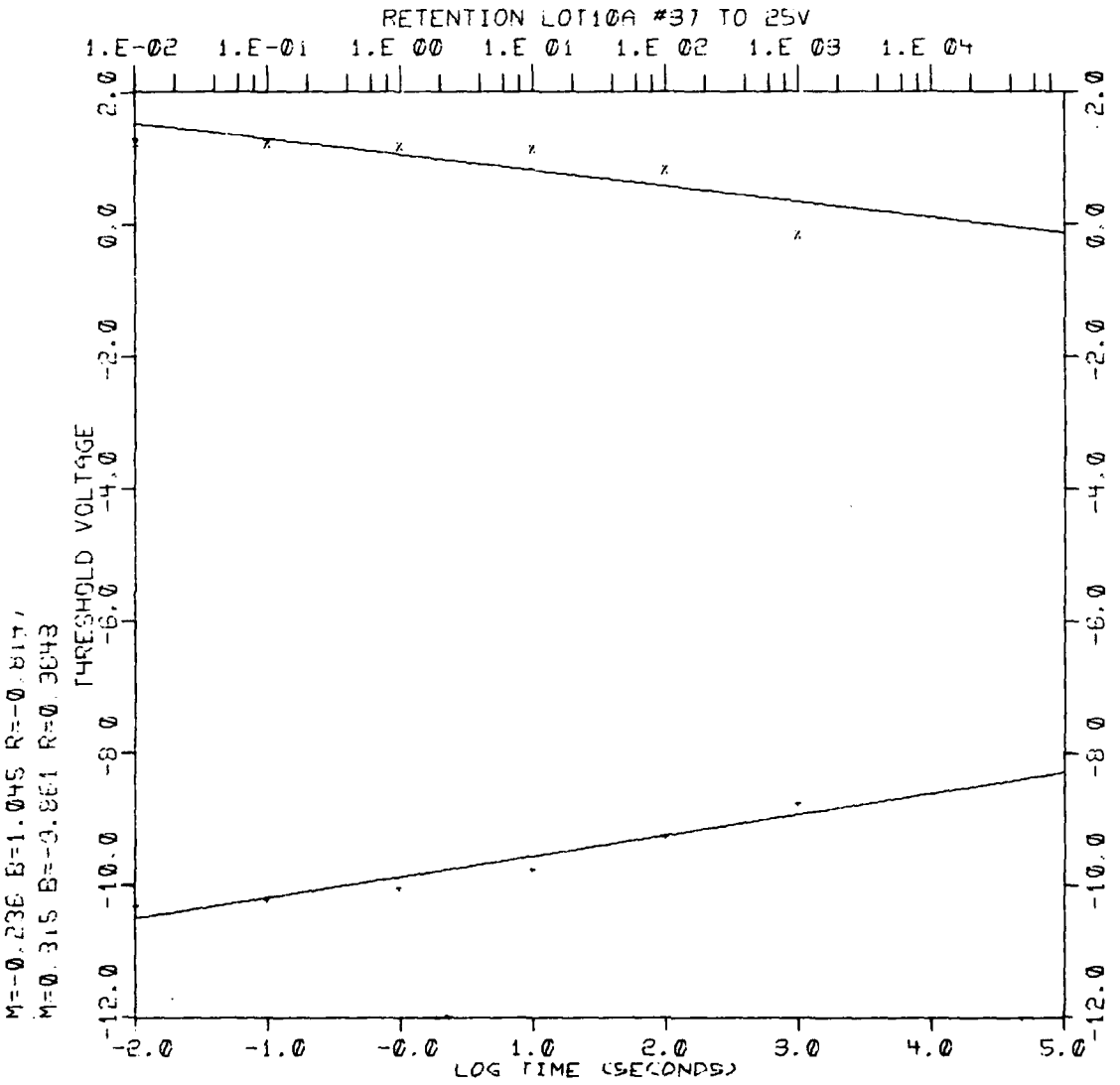

RETENTION LOT10A #37 TO 25V
1.E-02 1.E-01 1.E 00 1.E 01 1.E 02 1.E 03 1.E 04
THRESHOLD VOLTAGE
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-2.0 -1.0 -0.0 1.0 2.0 3.0 4.0 5.0
LOG TIME (SECONDS)
M=-0.236 B=1.045 R=-0.817
M=0.315 B=-3.861 R=0.3643

Fig. IV-65

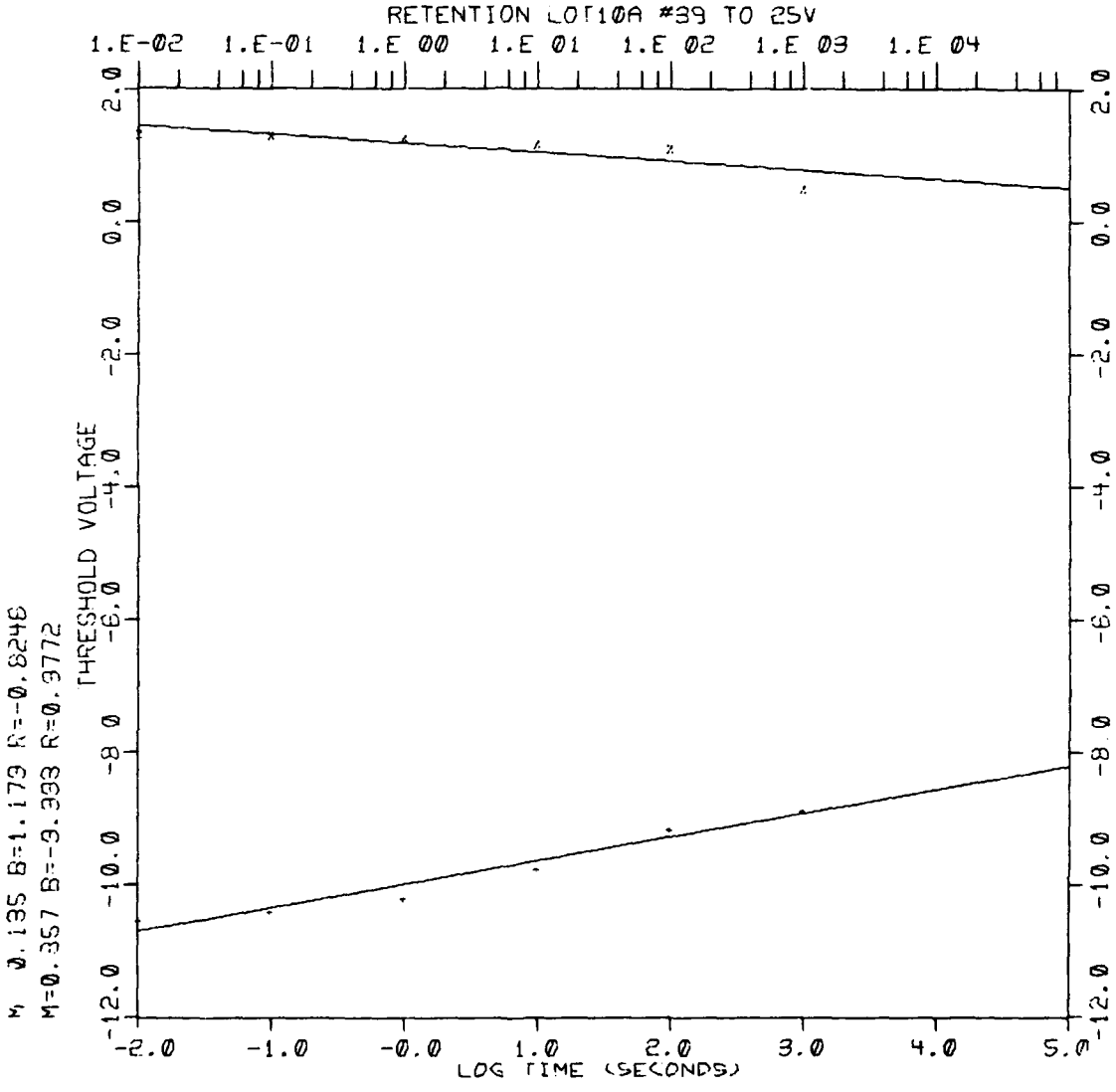

RETENTION LOT10A #39 TO 25V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
M1=0.357 B=-3.333 R=0.9772
M2 0.135 B=1.179 R=-0.8246
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)

Fig. IV- 66

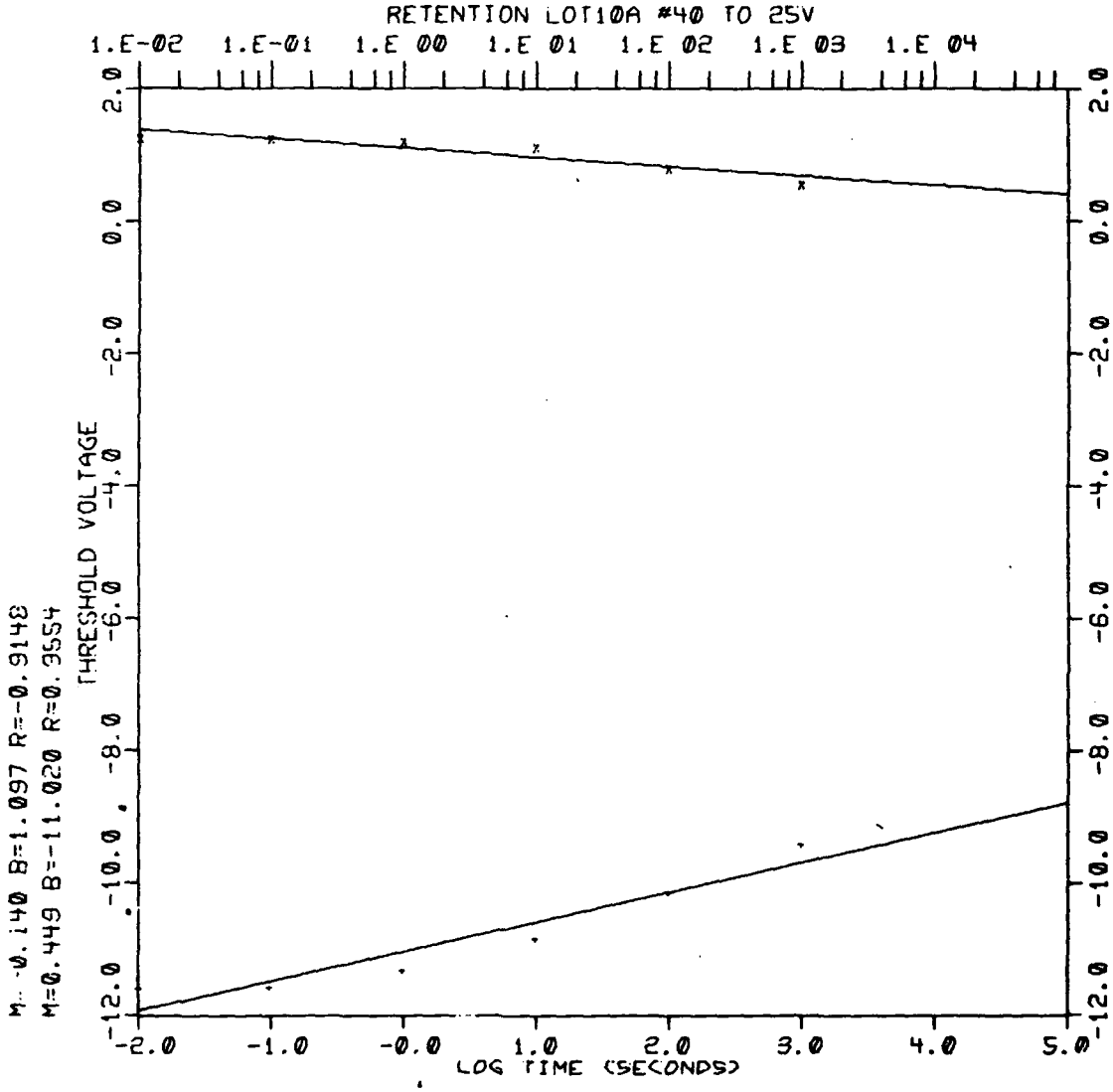

RETENTION LOT10A #40 TO 25V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
M=-0.1140 B=1.097 R=-0.9148
M=0.449 B=-11.020 R=0.9554
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)

Fig. IV-67

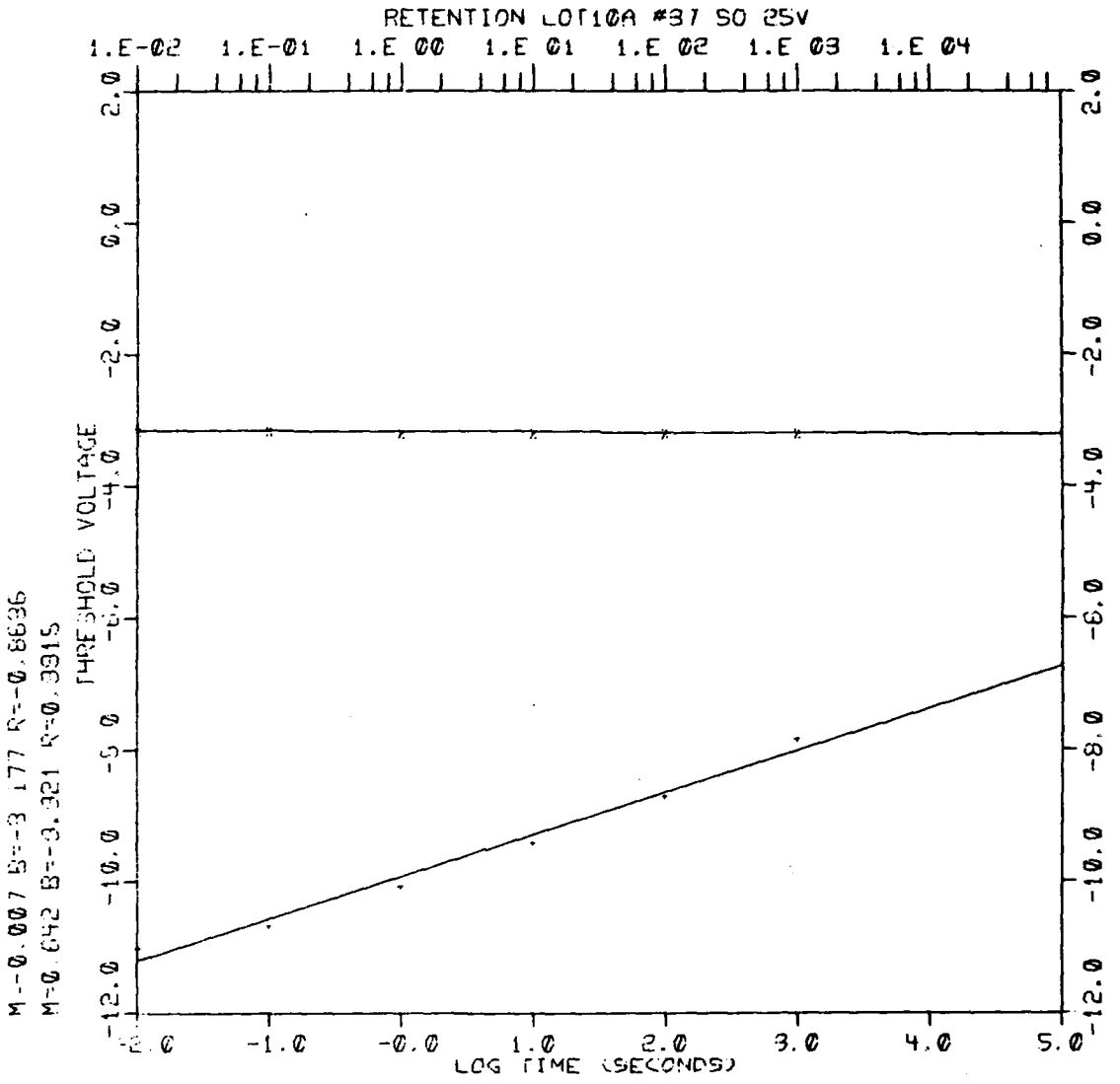

RETENTION LOT10A #37 SO 25V
1.E-02 1.E-01 1.E 00 1.E 01 1.E 02 1.E 03 1.E 04
THRESHOLD VOLTAGE
LOG TIME (SECONDS)
M=-0.007 B=-3.177 R=-0.8636
M=0.642 B=-3.321 R=0.3315

Fig. IV-68

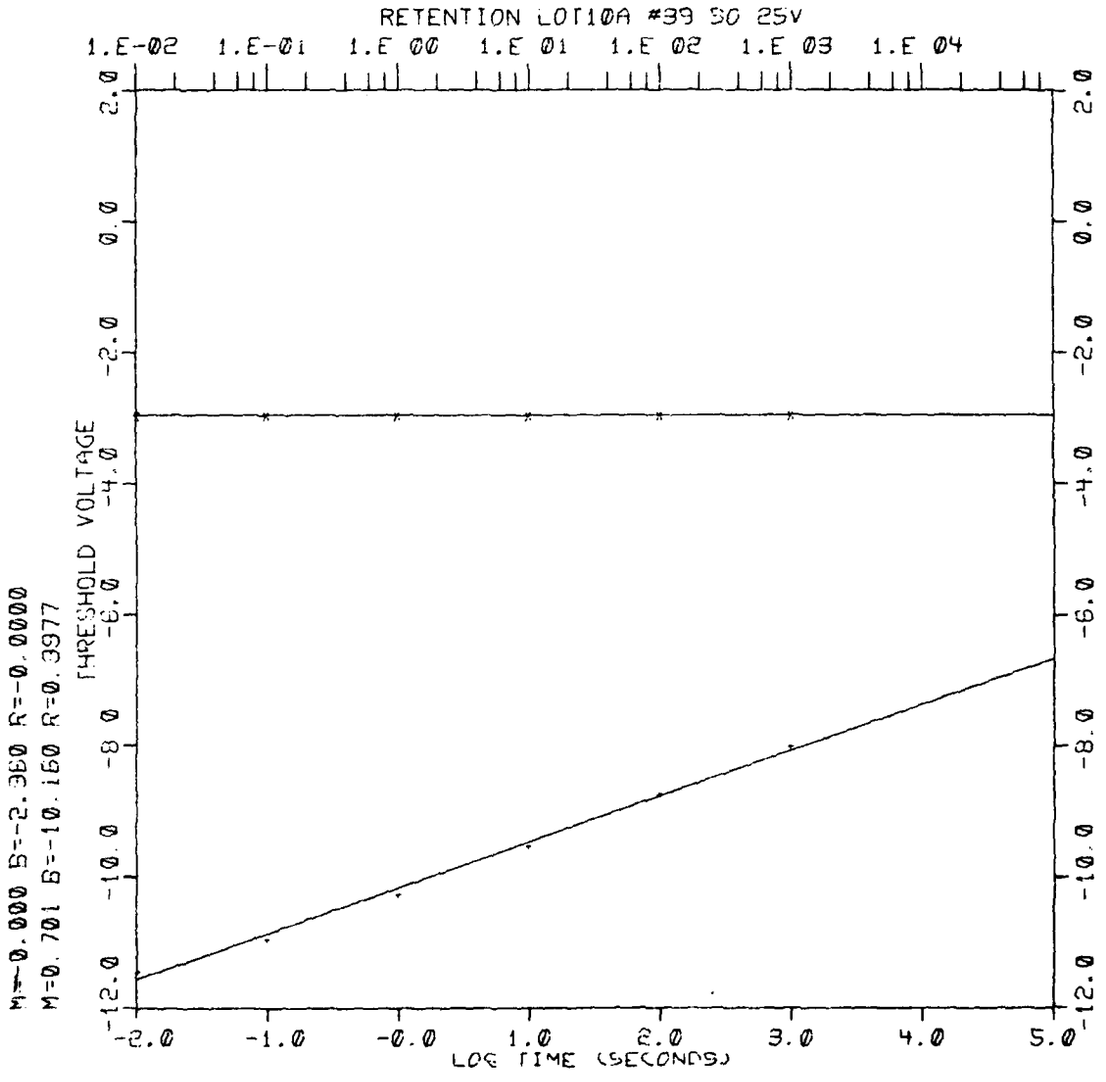

RETENTION LOT10A #39 50 25V
1.E-02 1.E-01 1.E 00 1.E 01 1.E 02 1.E 03 1.E 04
THRESHOLD VOLTAGE
LOG TIME (SECONDS)
M=-0.000 B=-2.360 R=-0.0000
M=0.701 B=-10.160 R=0.3977

Fig. IV-69

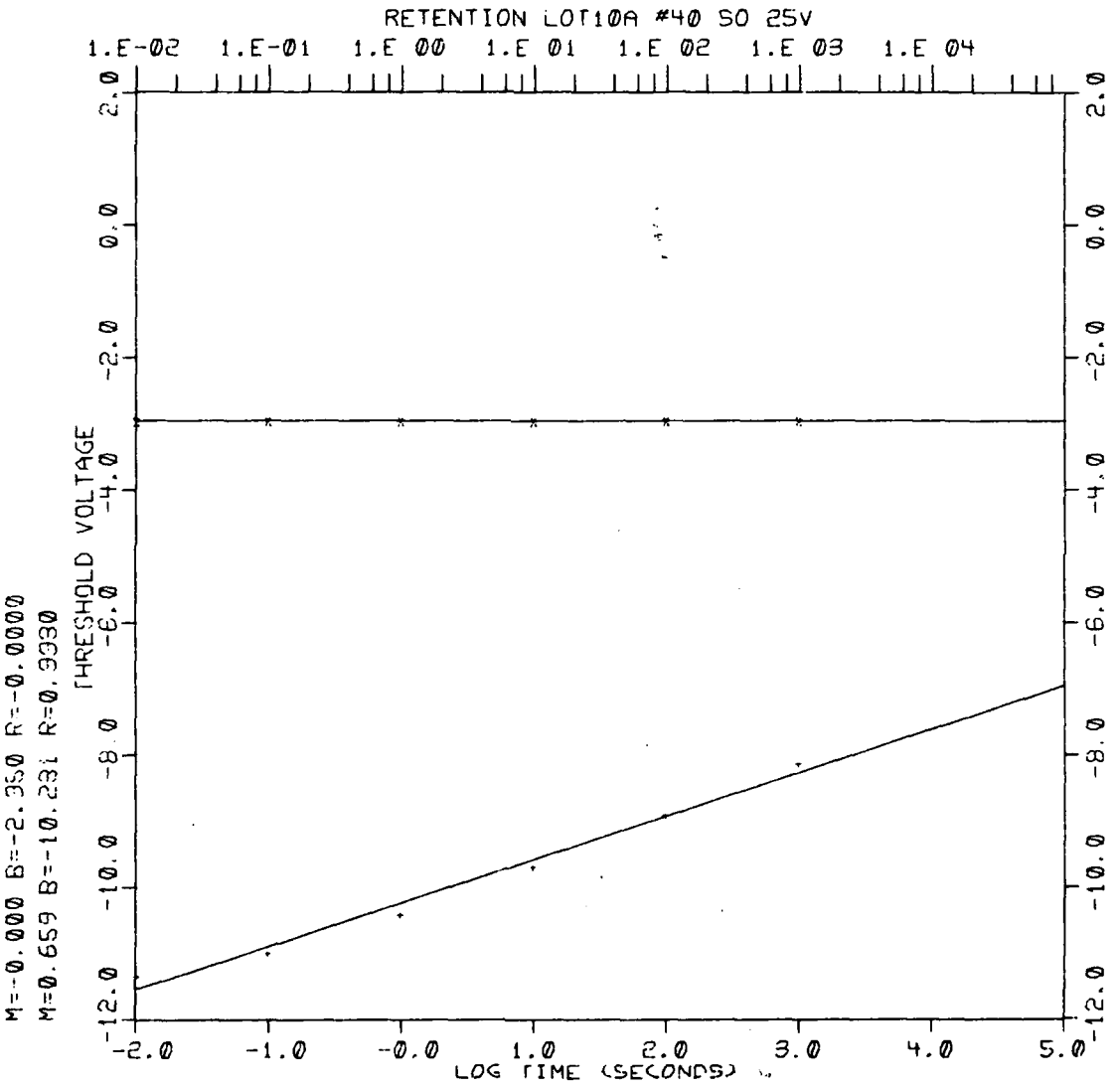

RETENTION LOT10A #40 SO 25V
1.E-02 1.E-01 1.E 00 1.E 01 1.E 02 1.E 03 1.E 04
THRESHOLD VOLTAGE
LOG TIME (SECONDS)
M=-0.000 B=-2.350 R=-0.0000
M=0.659 B=-10.231 R=0.9330

Fig. IV-70

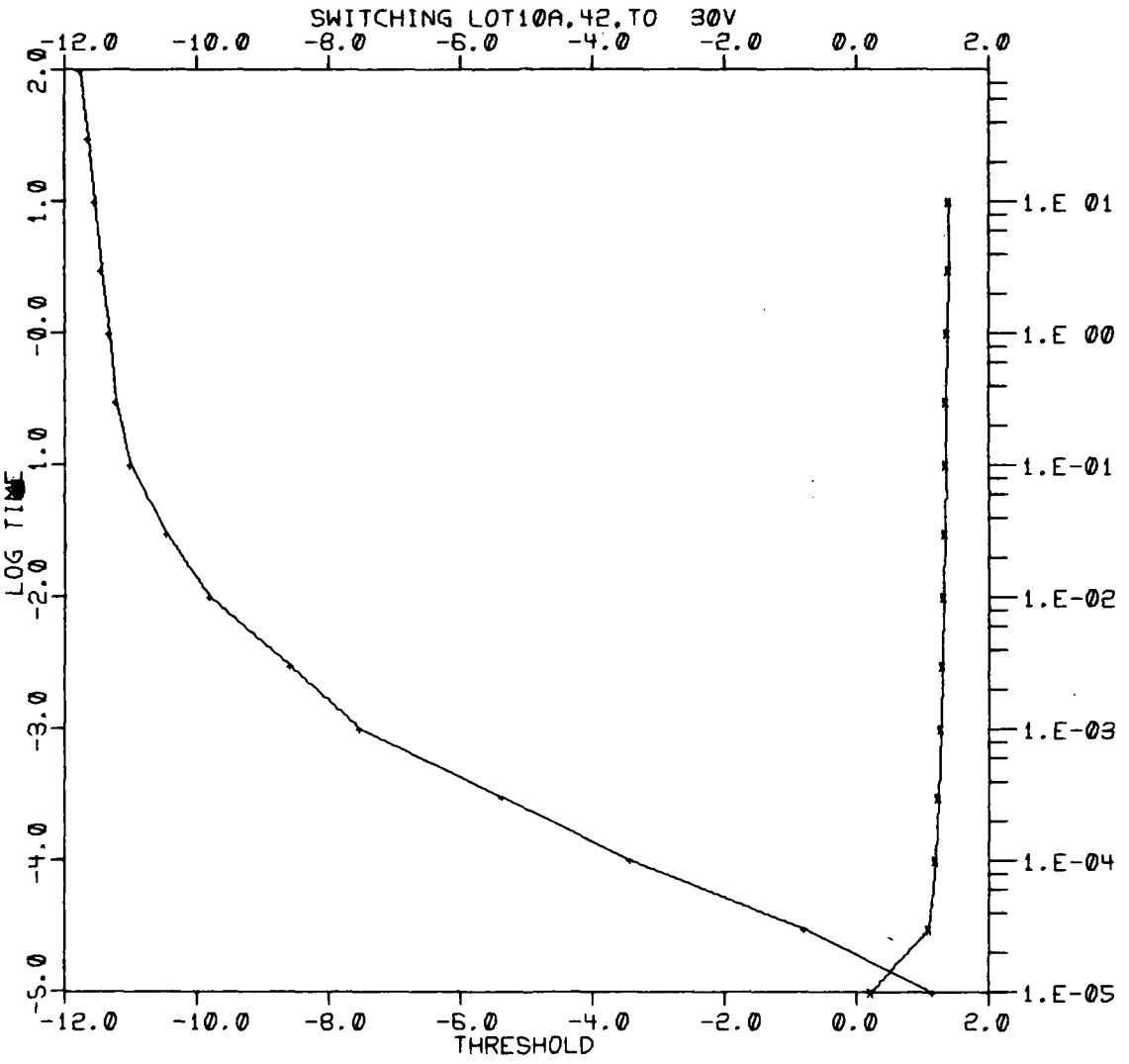

SWITCHING LOT10A,42,TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-71

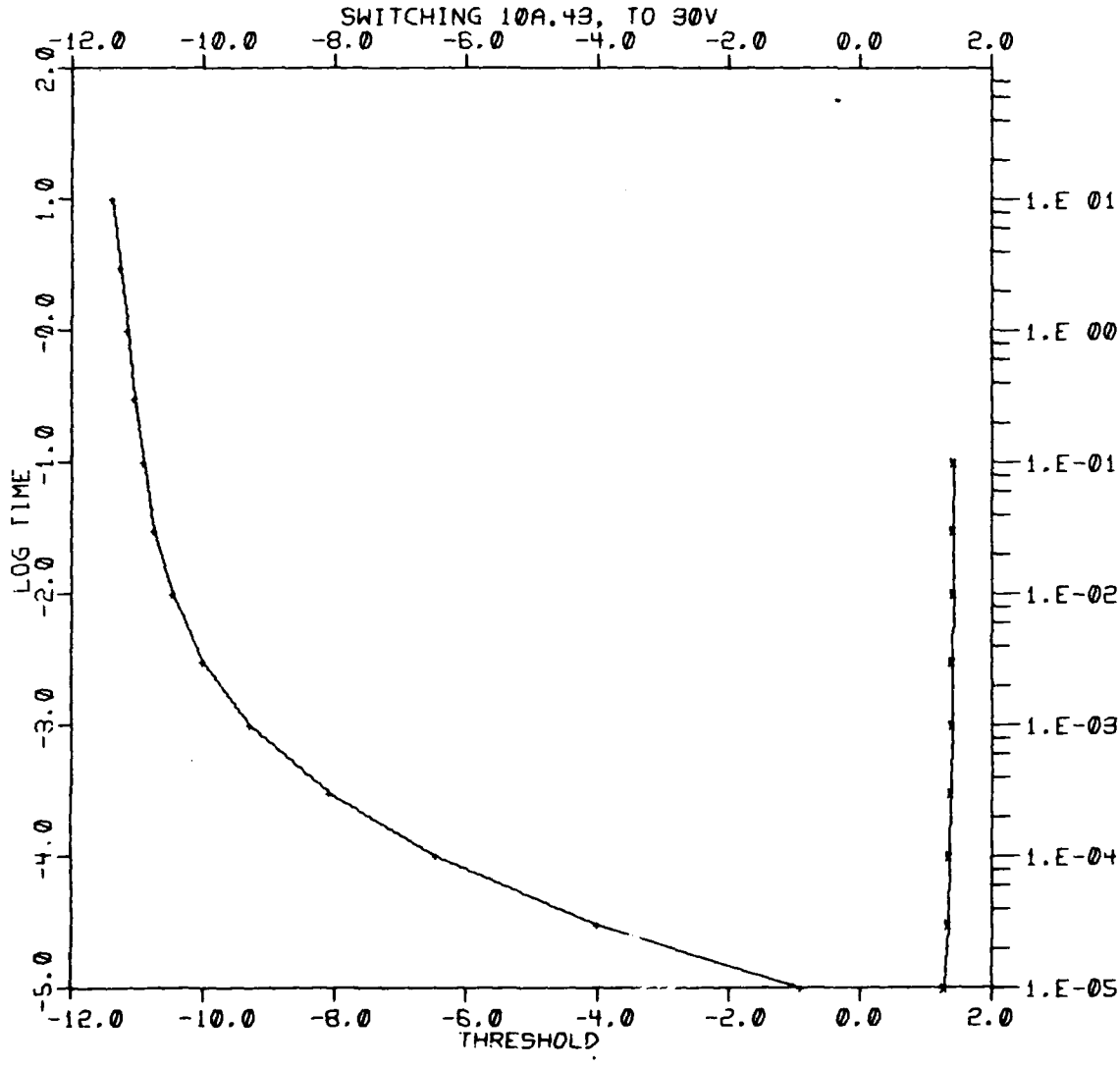

SWITCHING 10A.43, TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-72

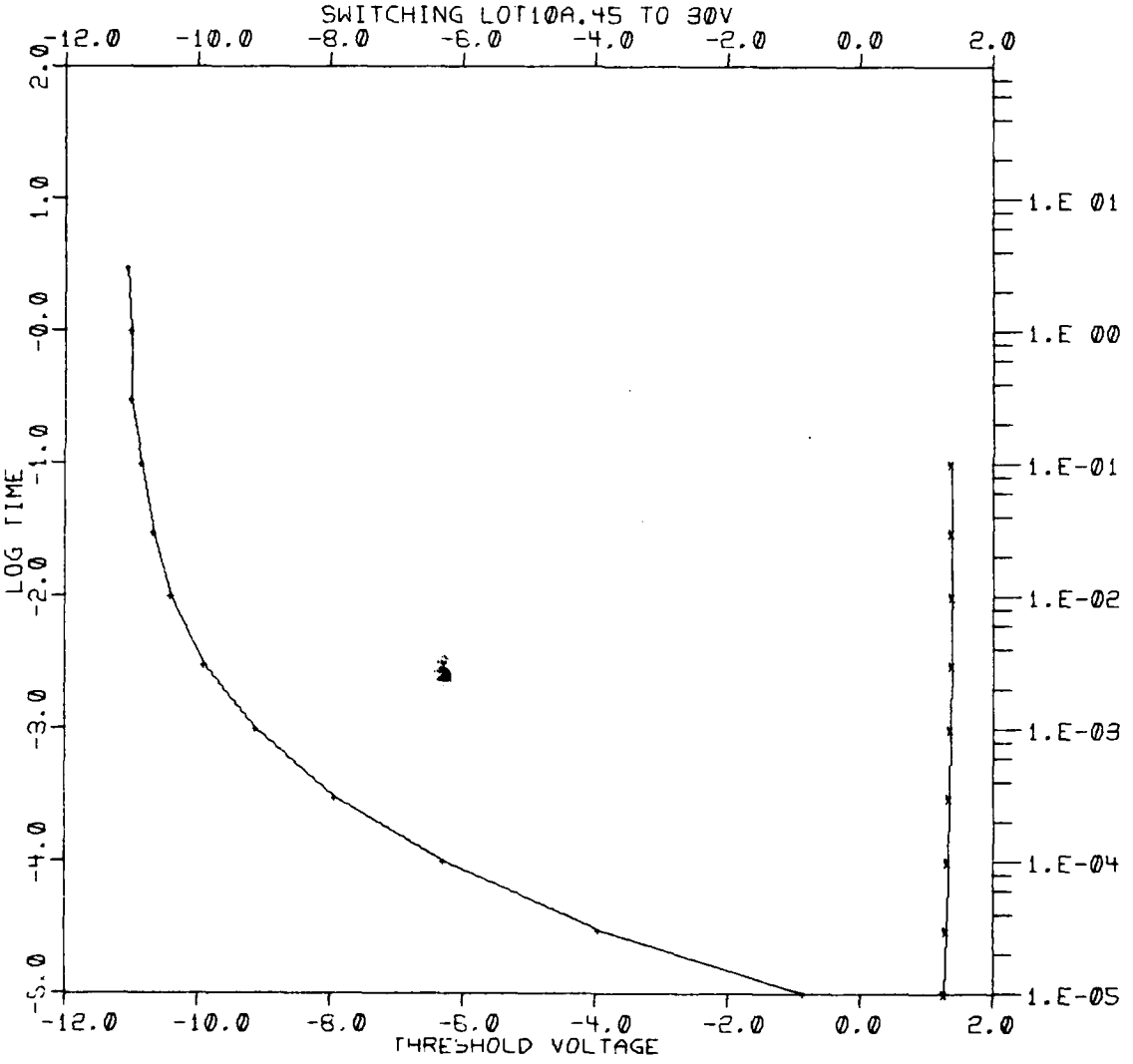

SWITCHING LOT10A.45 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-73

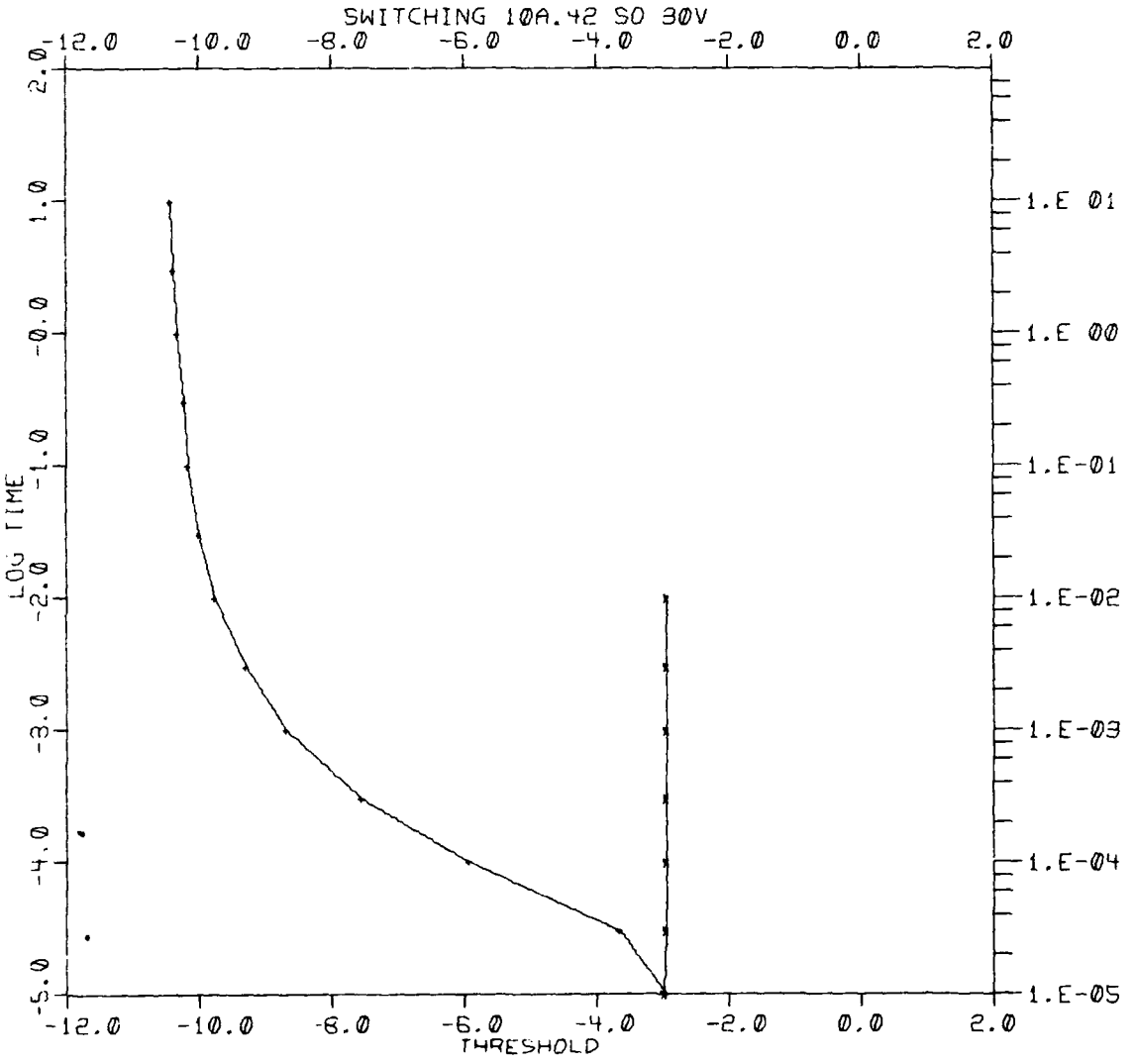

SWITCHING 10A.42 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-74

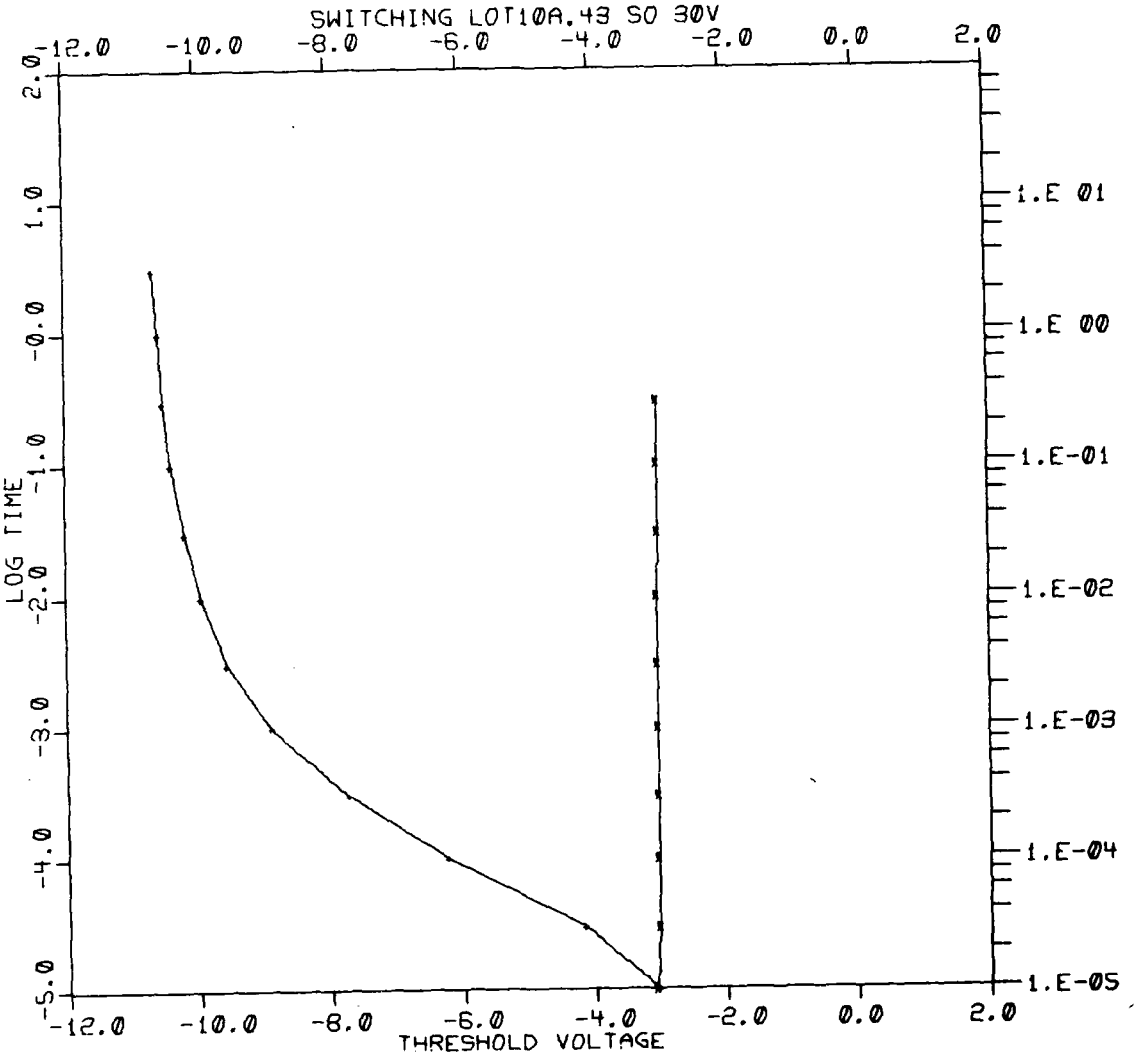

SWITCHING LOT10A.43 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-75

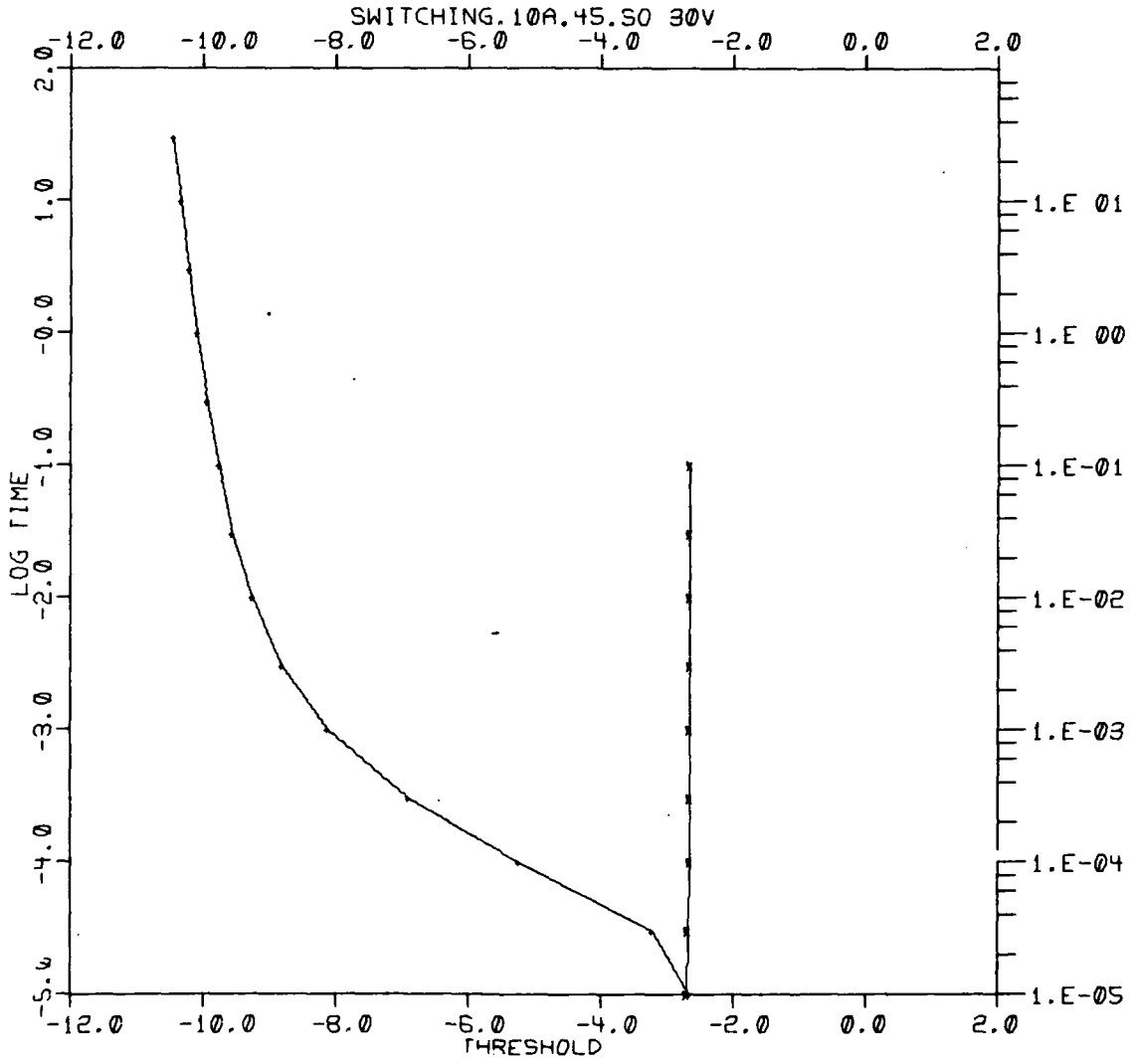

SWITCHING.10A.45.SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-76

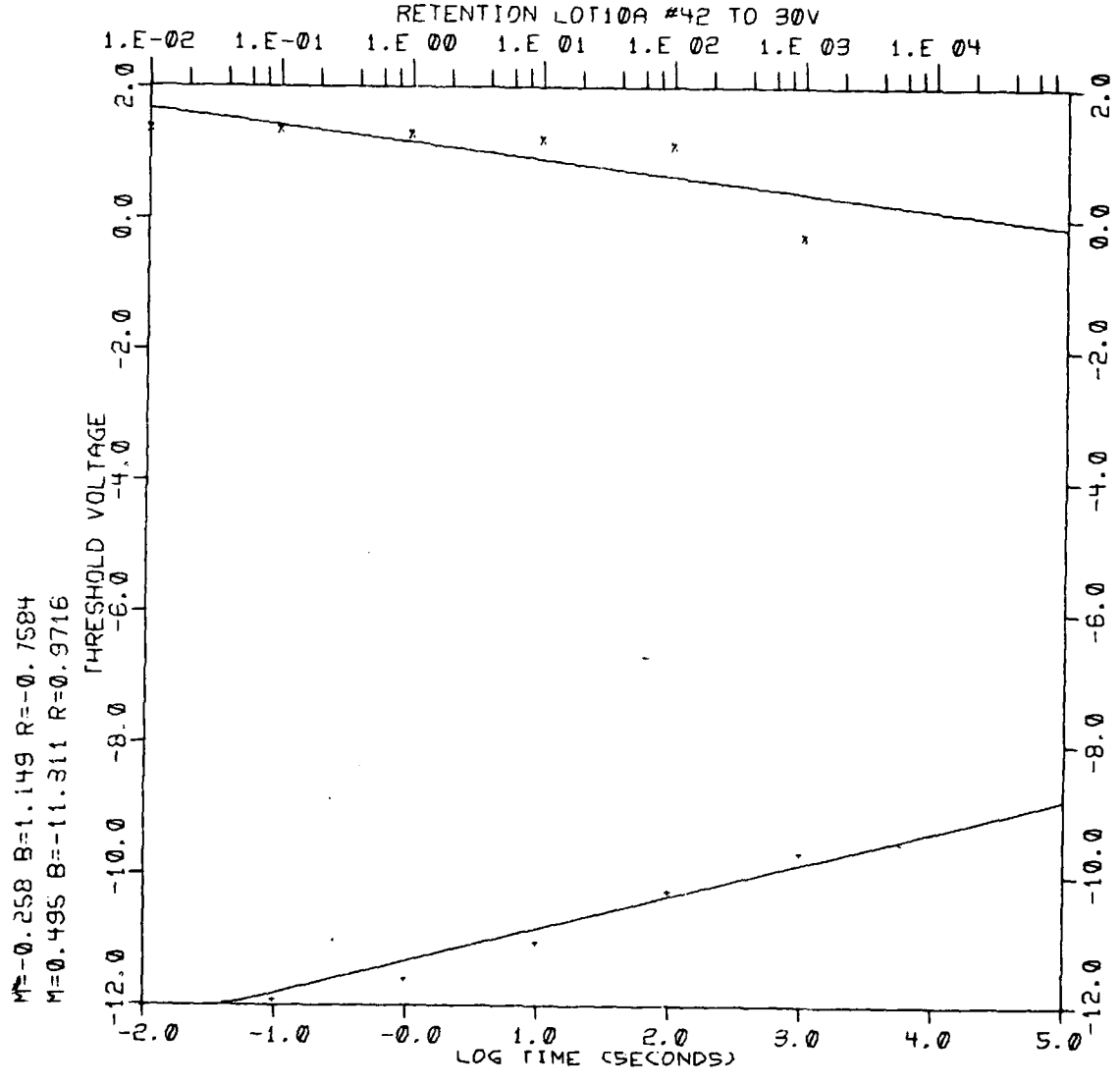

RETENTION LOT10A #42 TO 30V
1.E-02 1.E-01 1.E 00 1.E 01 1.E 02 1.E 03 1.E 04
THRESHOLD VOLTAGE
LOG TIME (SECONDS)
M=-0.258 B=1.149 R=-0.7584
M=0.495 B=-11.311 R=0.9716

Fig. IV-77

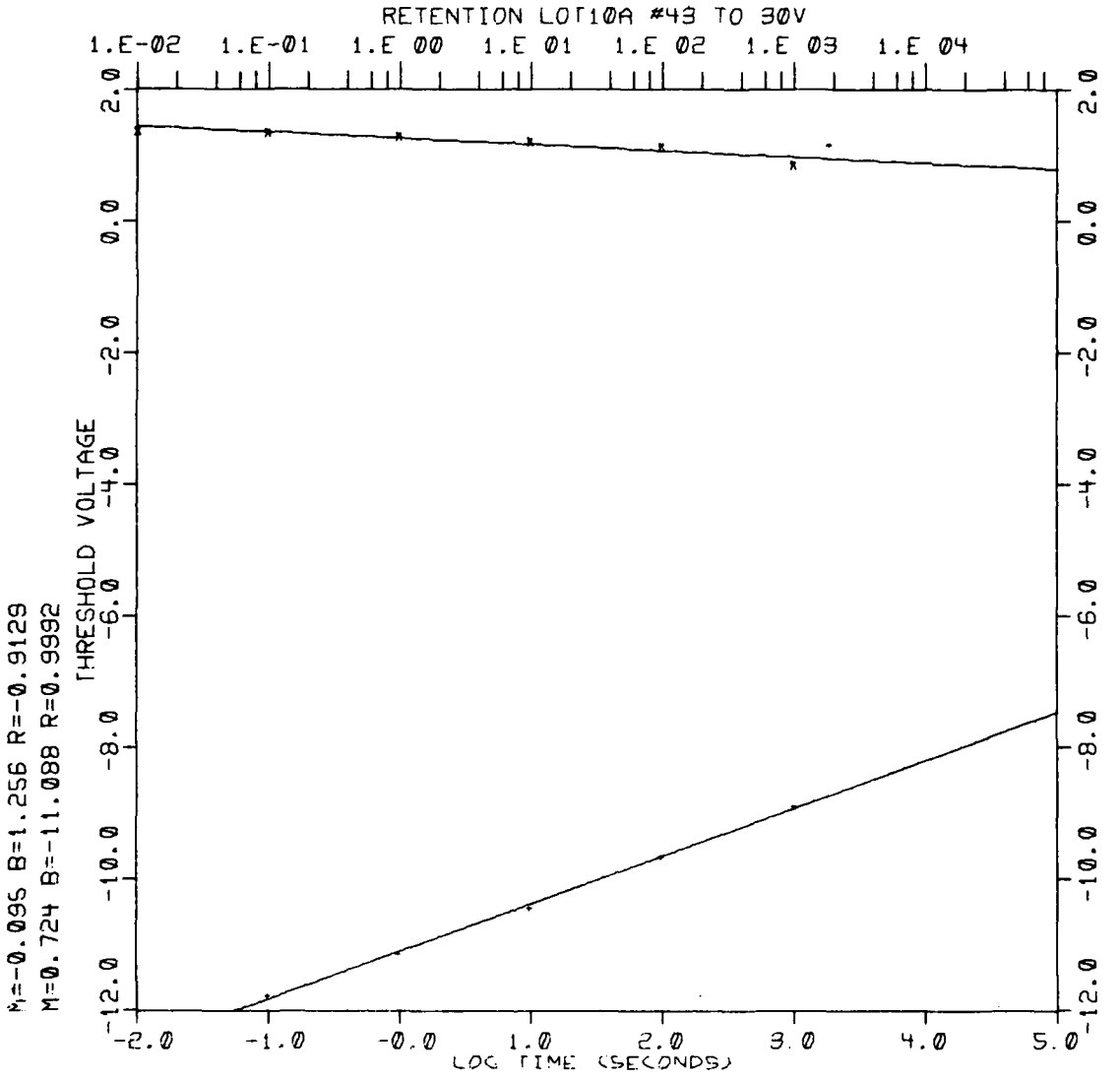

RETENTION LOT10A #43 TO 30V
1.E-02 1.E-01 1.E 00 1.E 01 1.E 02 1.E 03 1.E 04
THRESHOLD VOLTAGE
2.0 0.0 -2.0 -4.0 -6.0 -8.0 -10.0 -12.0
M=-0.095 B=1.256 R=-0.9129
M=0.724 B=-11.088 R=0.9992
-2.0 -1.0 -0.0 1.0 2.0 3.0 4.0 5.0
LOG TIME (SECONDS)

Fig. IV-78

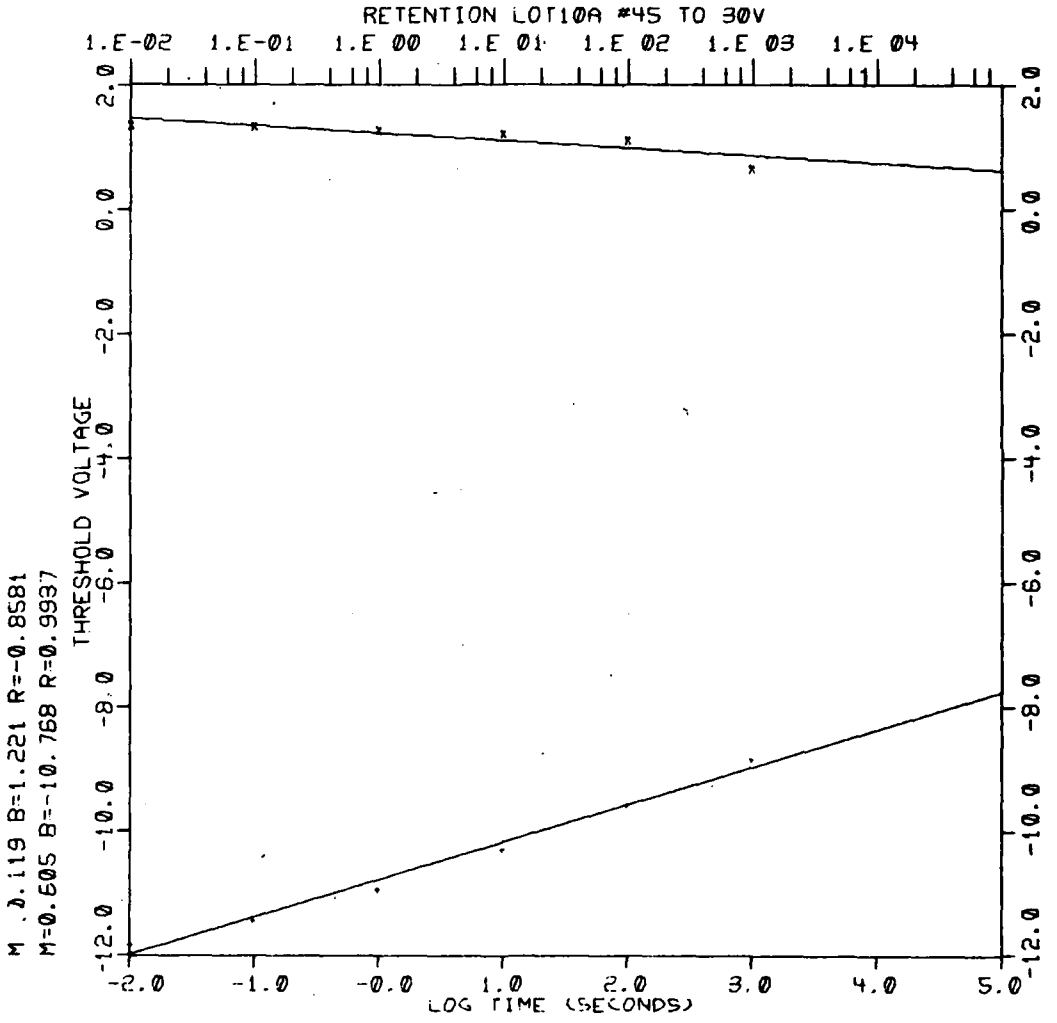

RETENTION LOT10A #45 TO 30V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
M =0.119 B=1.221 R=-0.8581
M=0.605 B=-10.768 R=0.9937
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)

Fig. IV-79

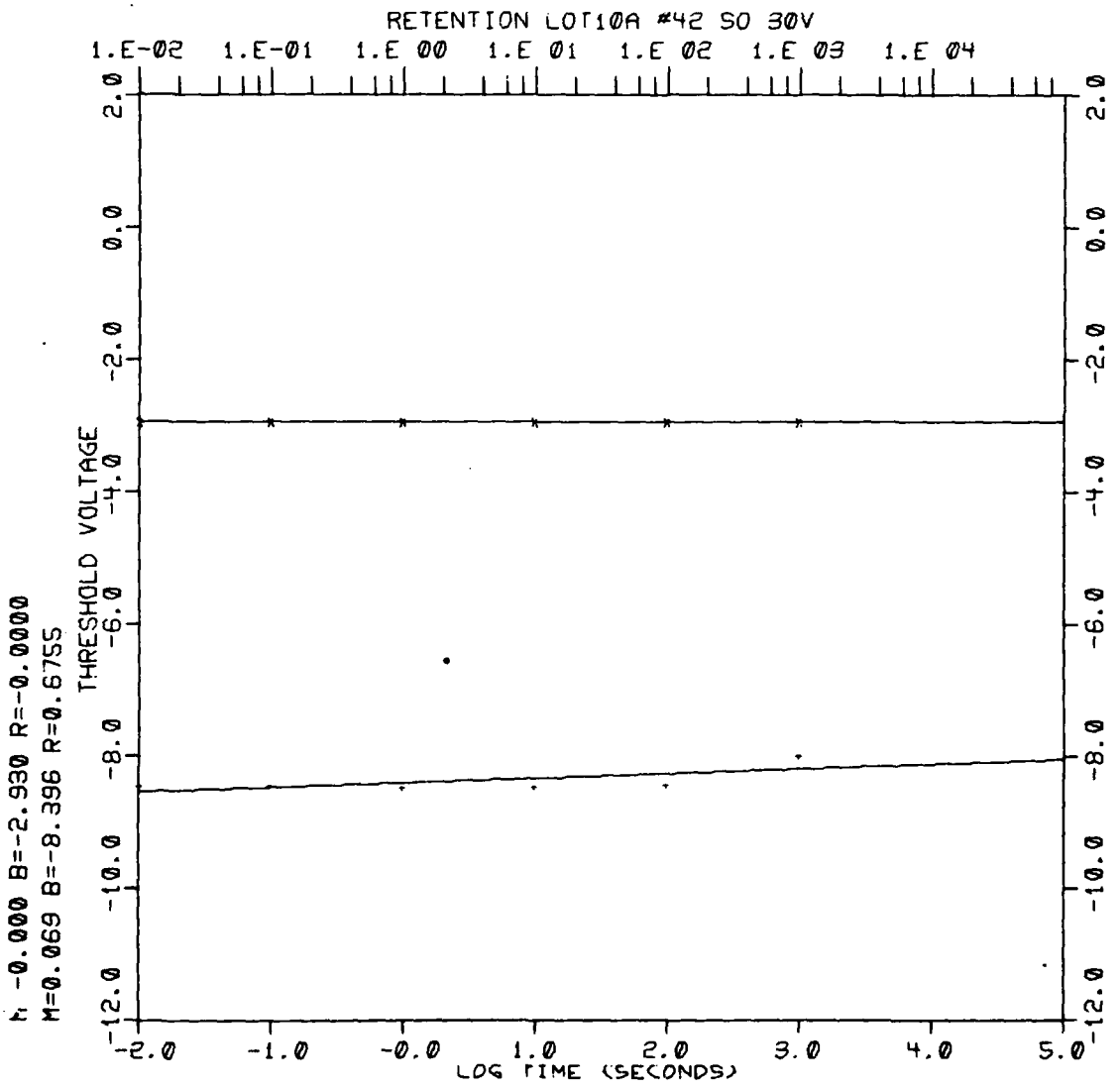

RETENTION LOT10A #42 SO 30V
1.E-02
1.E-01
1.E 00
1.E 01
1.E 02
1.E 03
1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
-2.0
-1.0
-0.0
1.0
2.0
3.0
4.0
5.0
LOG TIME (SECONDS)
M=0.069 B=-8.396 R=0.675S
-0.000 B=-2.930 R=-0.0000

Fig. IV-80

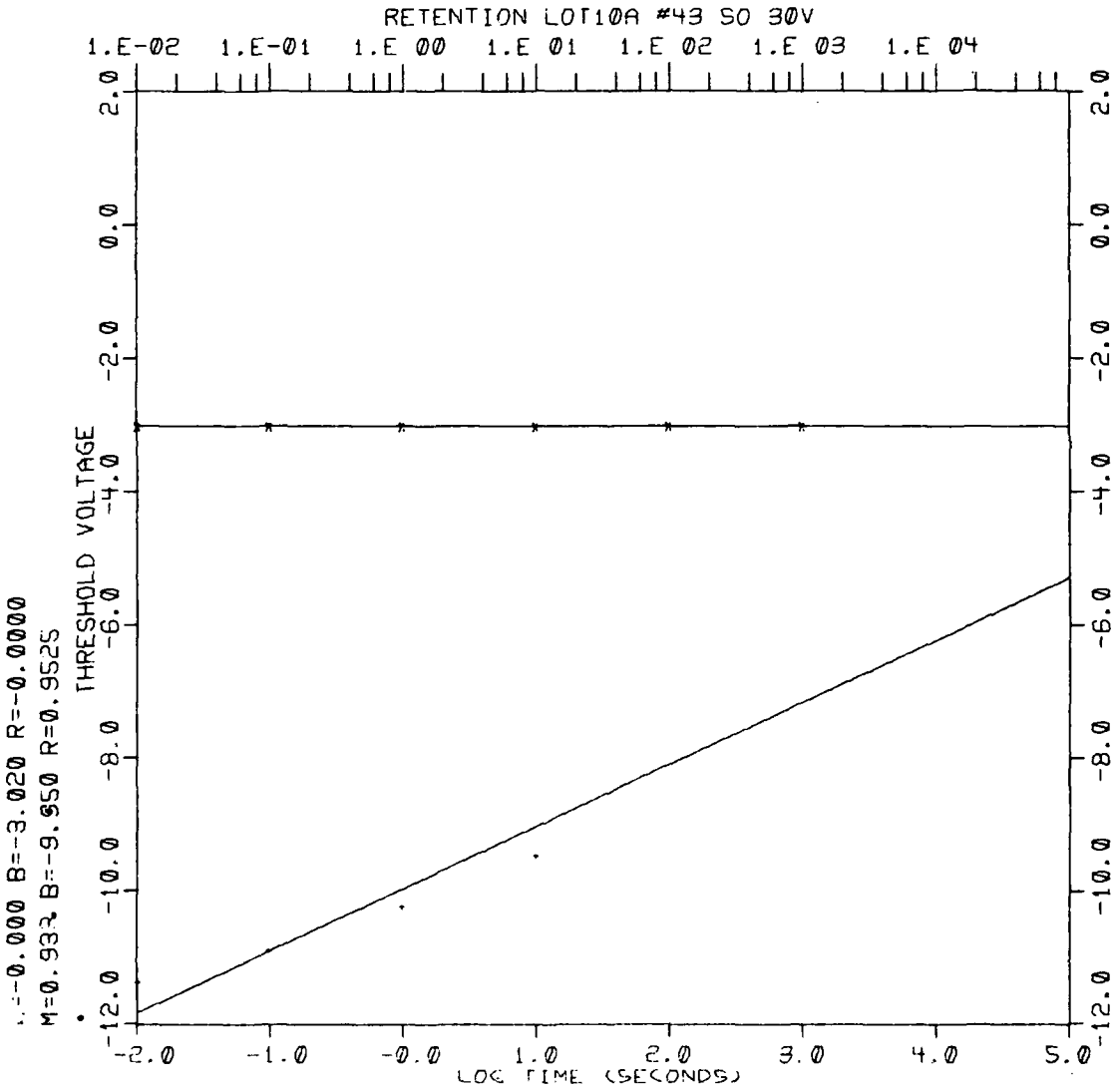

RETENTION LOT10A #43 SO 30V
1.E-02 1.E-01 1.E 00 1.E 01 1.E 02 1.E 03 1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
-2.0 -1.0 -0.0 1.0 2.0 3.0 4.0 5.0
LOG TIME (SECONDS)
M=0.932 B=-9.950 R=0.9525

Fig. IV-81

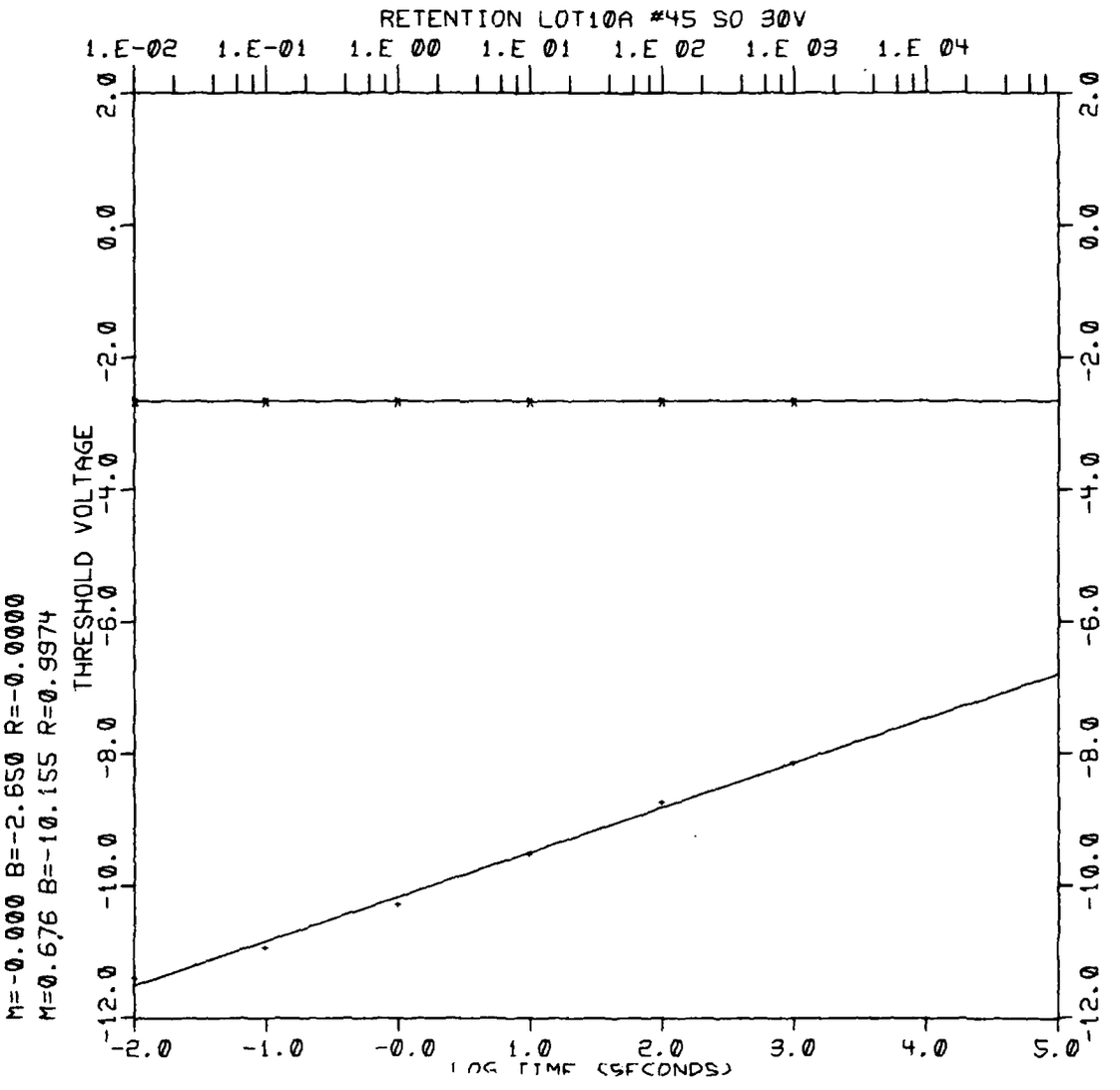

RETENTION LOT10A #45 SO 30V
1.E-02 1.E-01 1.E 00 1.E 01 1.E 02 1.E 03 1.E 04
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
THRESHOLD VOLTAGE
M=-0.000 B=-2.650 R=-0.0000
M=0.676 B=-10.155 R=0.9974
-2.0 -1.0 -0.0 1.0 2.0 3.0 4.0 5.0
LOG TIME (SECONDS)

Fig. IV-82

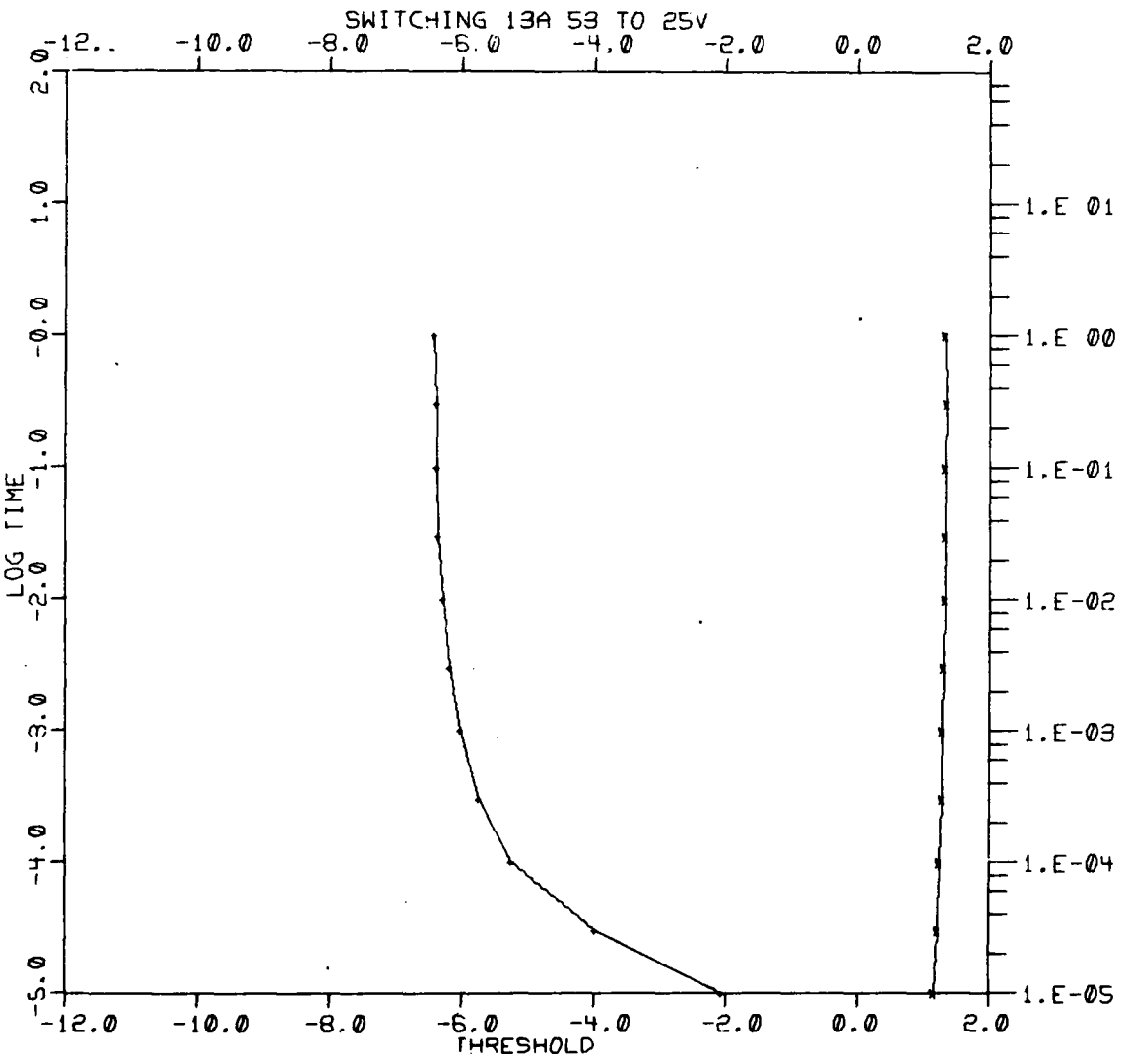

SWITCHING 13A 53 TO 25V
-12..
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
THRESHOLD

Fig. IV-83

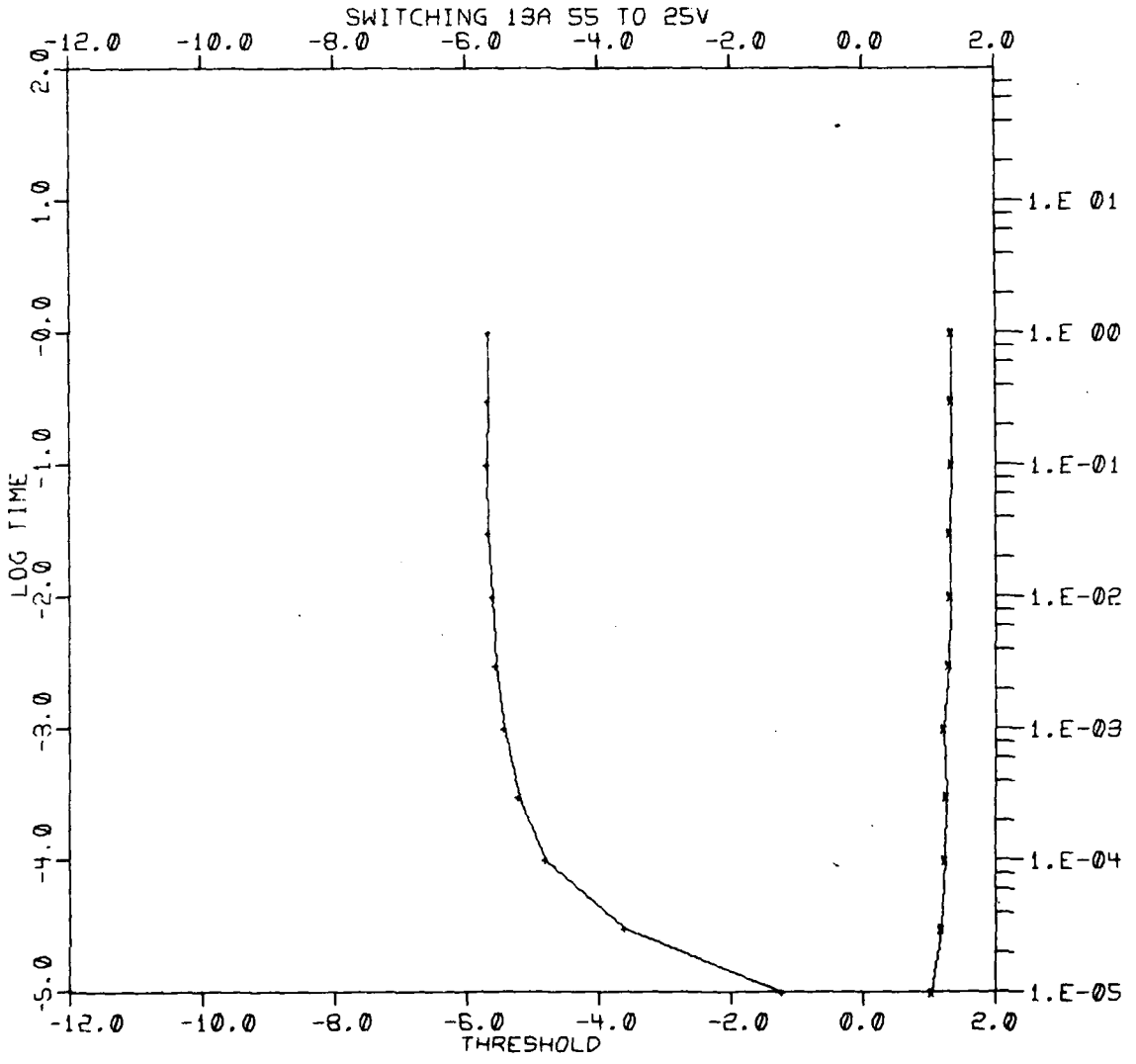

SWITCHING 13A 55 TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-84

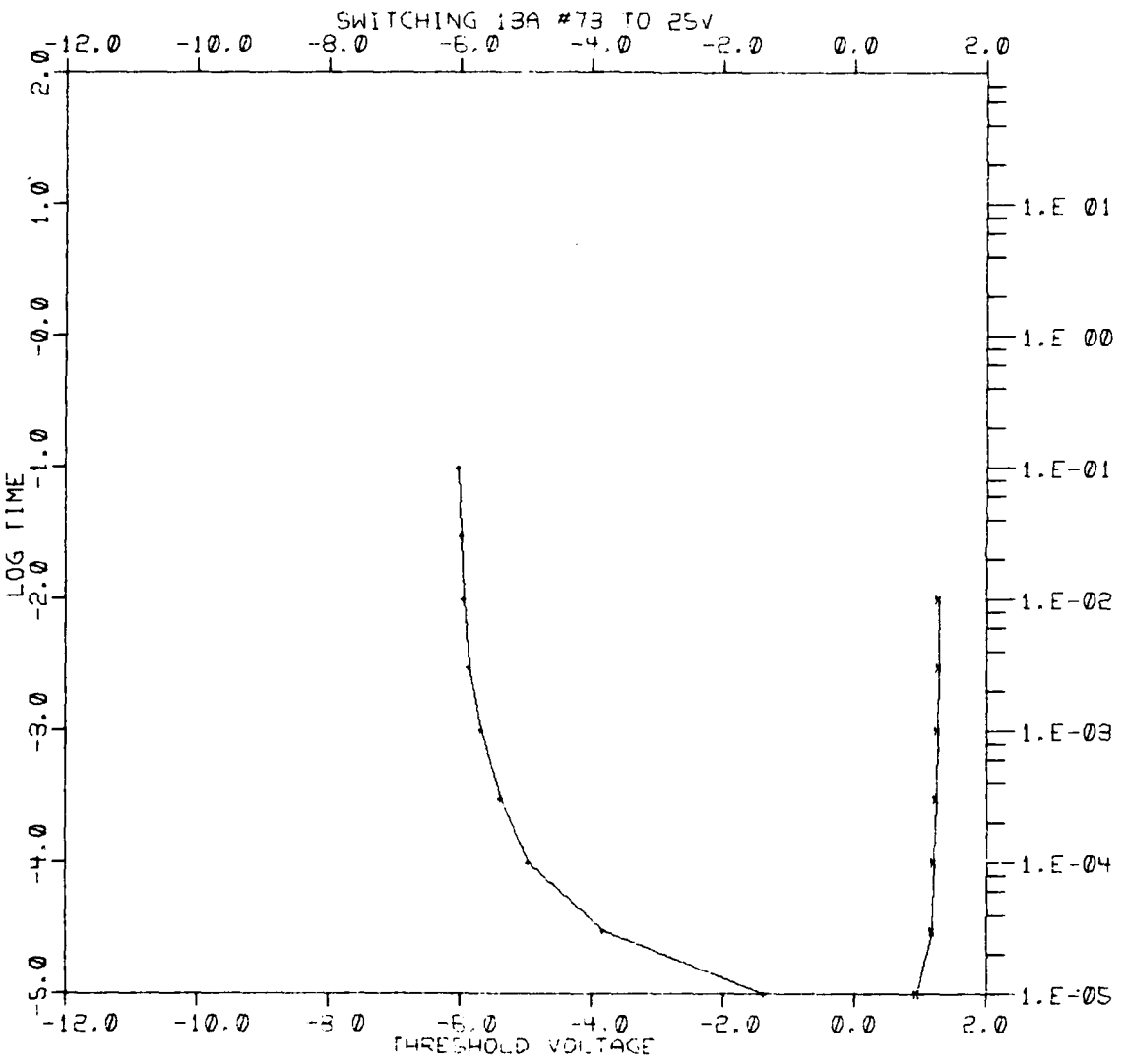

SWITCHING 13A #73 TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-85

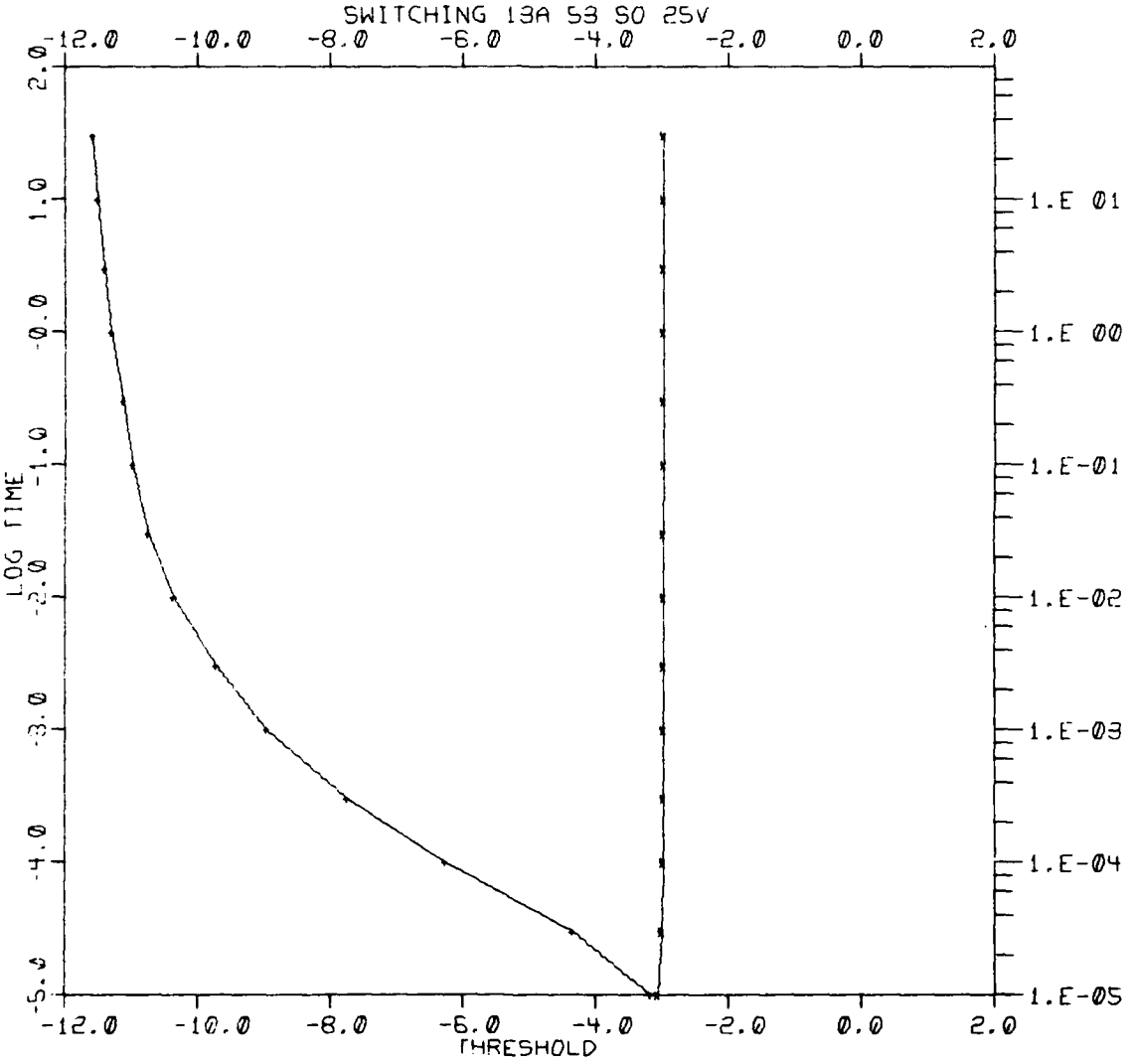

SWITCHING 13A 53 SO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-86

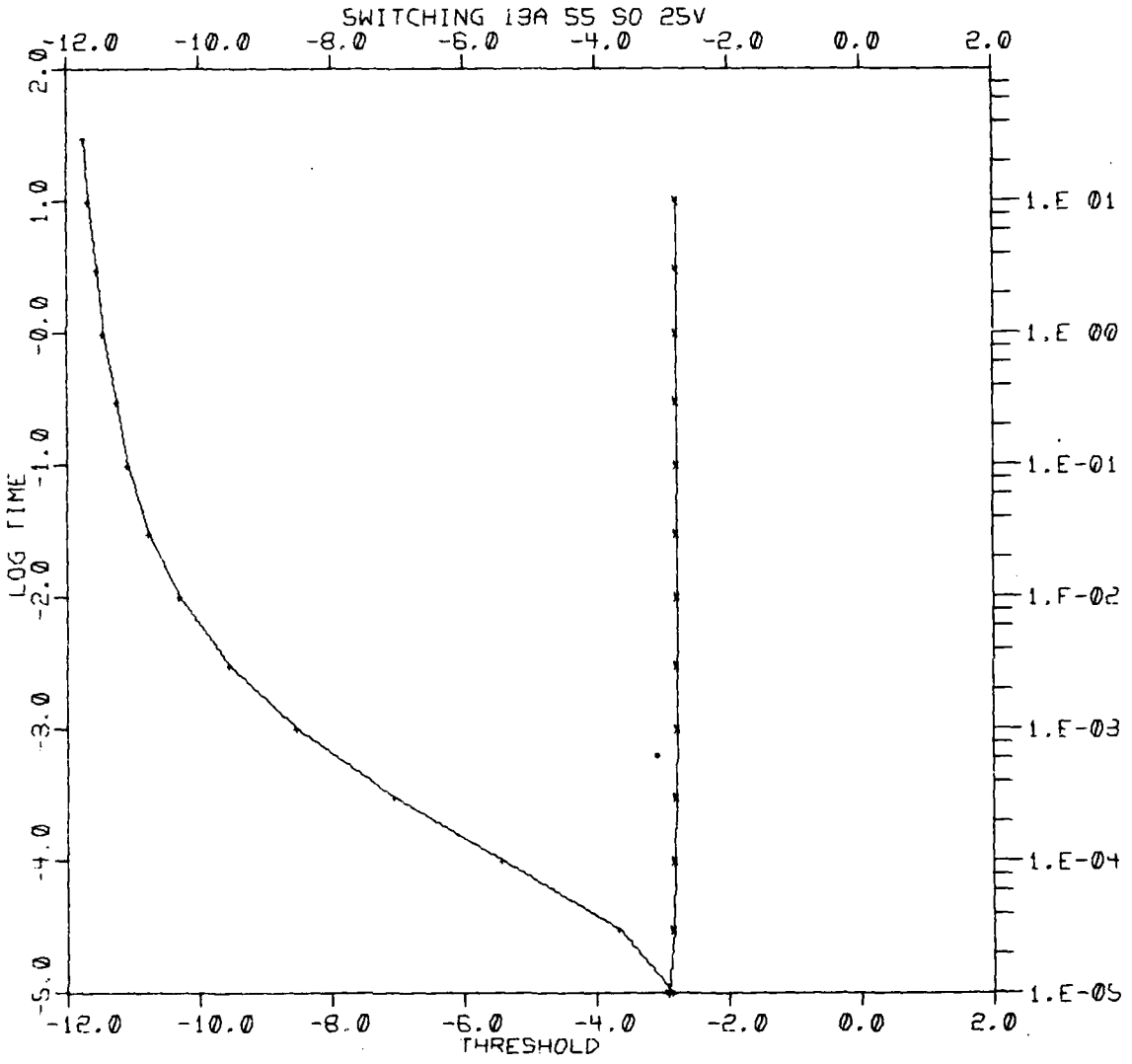

SWITCHING 13A 55 SO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-87

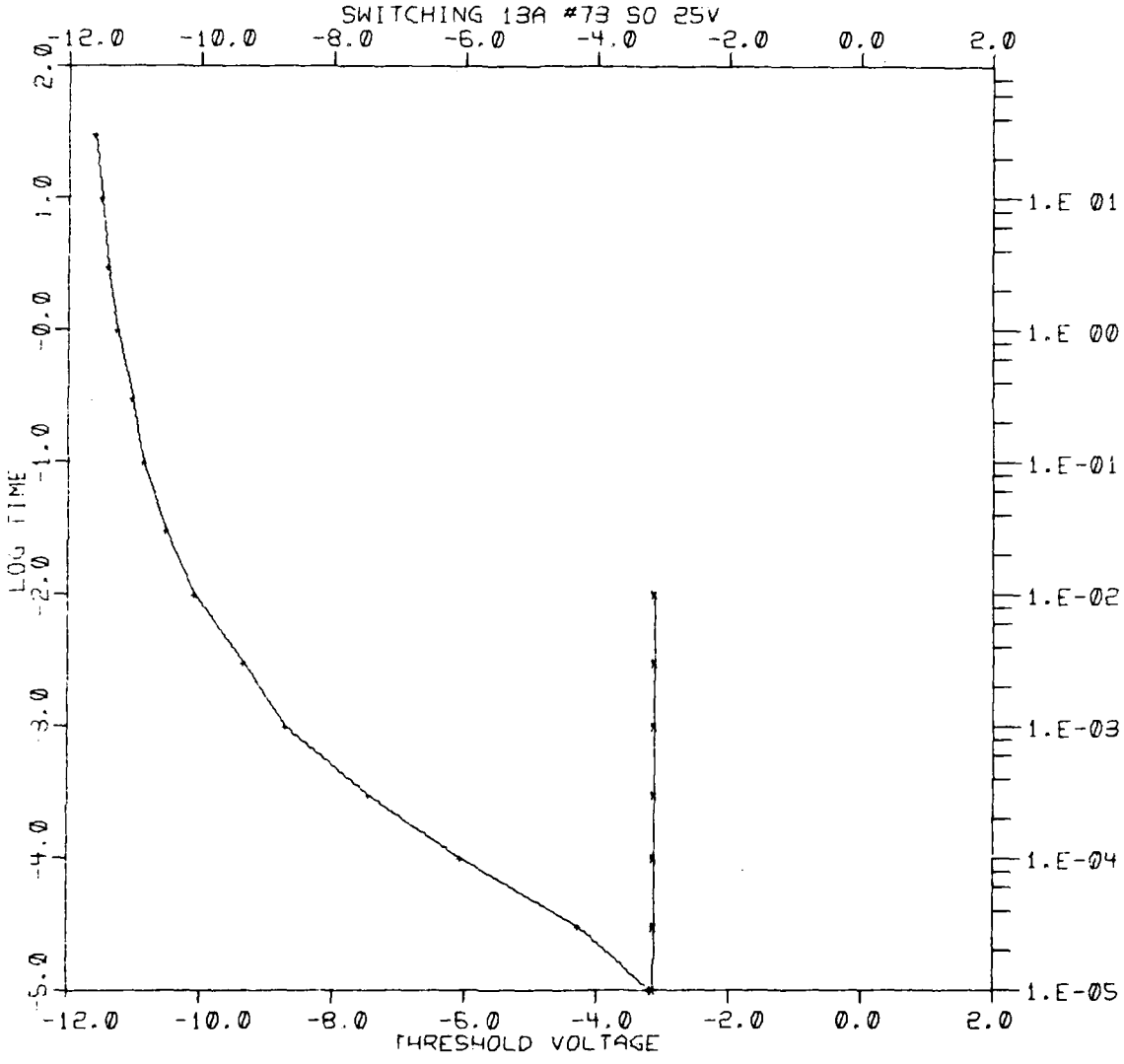

SWITCHING 13A #73 SO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-88

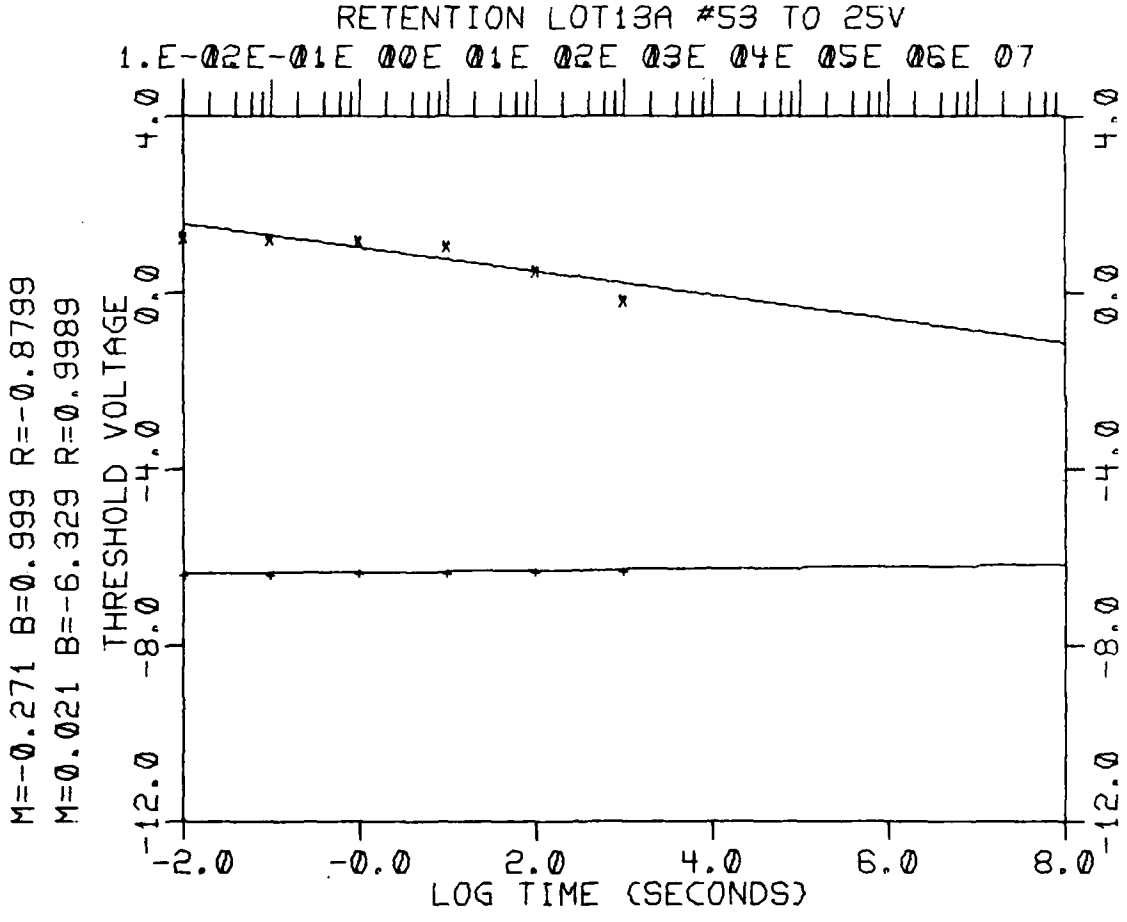

RETENTION LOT13A #53 TO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.271 B=0.999 R=-0.8799
M=0.021 B=-6.329 R=0.9989
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-89

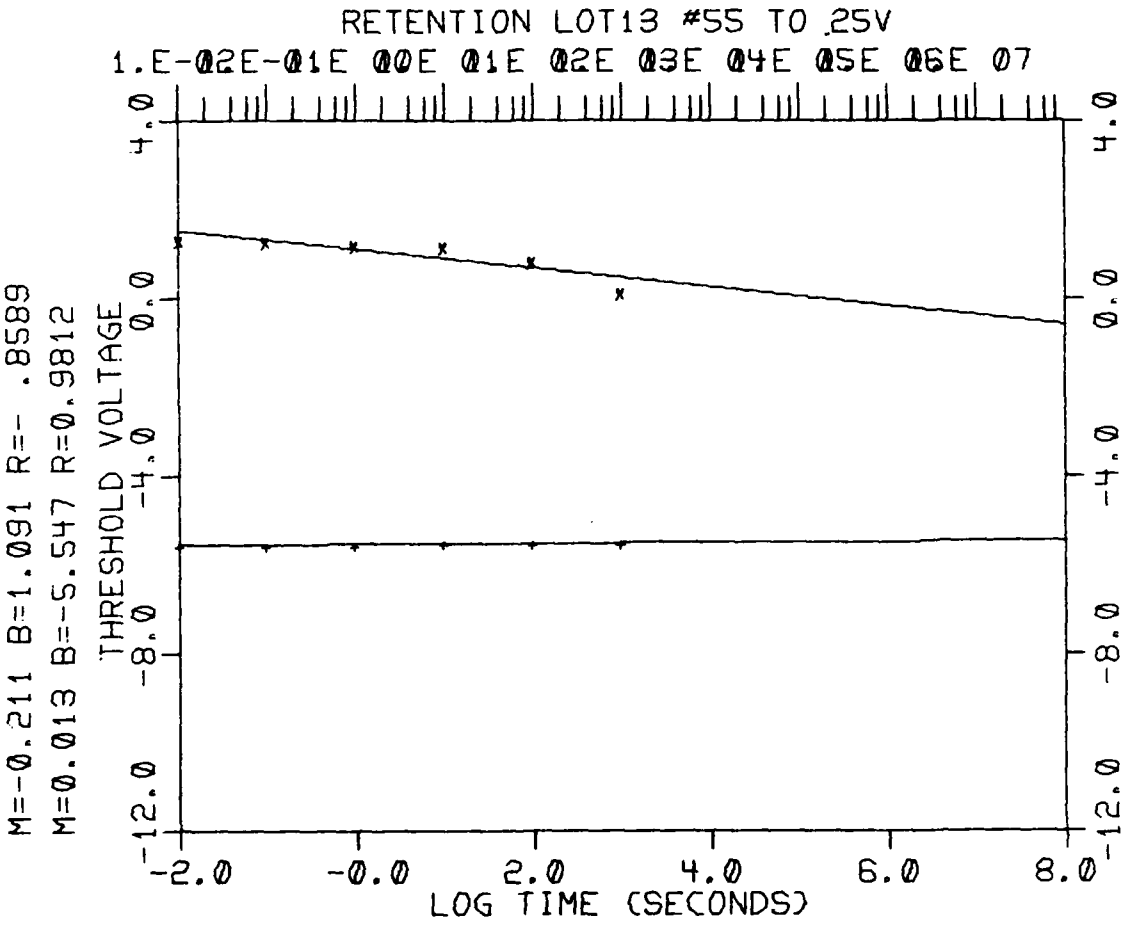

RETENTION LOT13 #55 TO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.211 B=1.091 R=- .8589
M=0.013 B=-5.547 R=0.9812
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-90

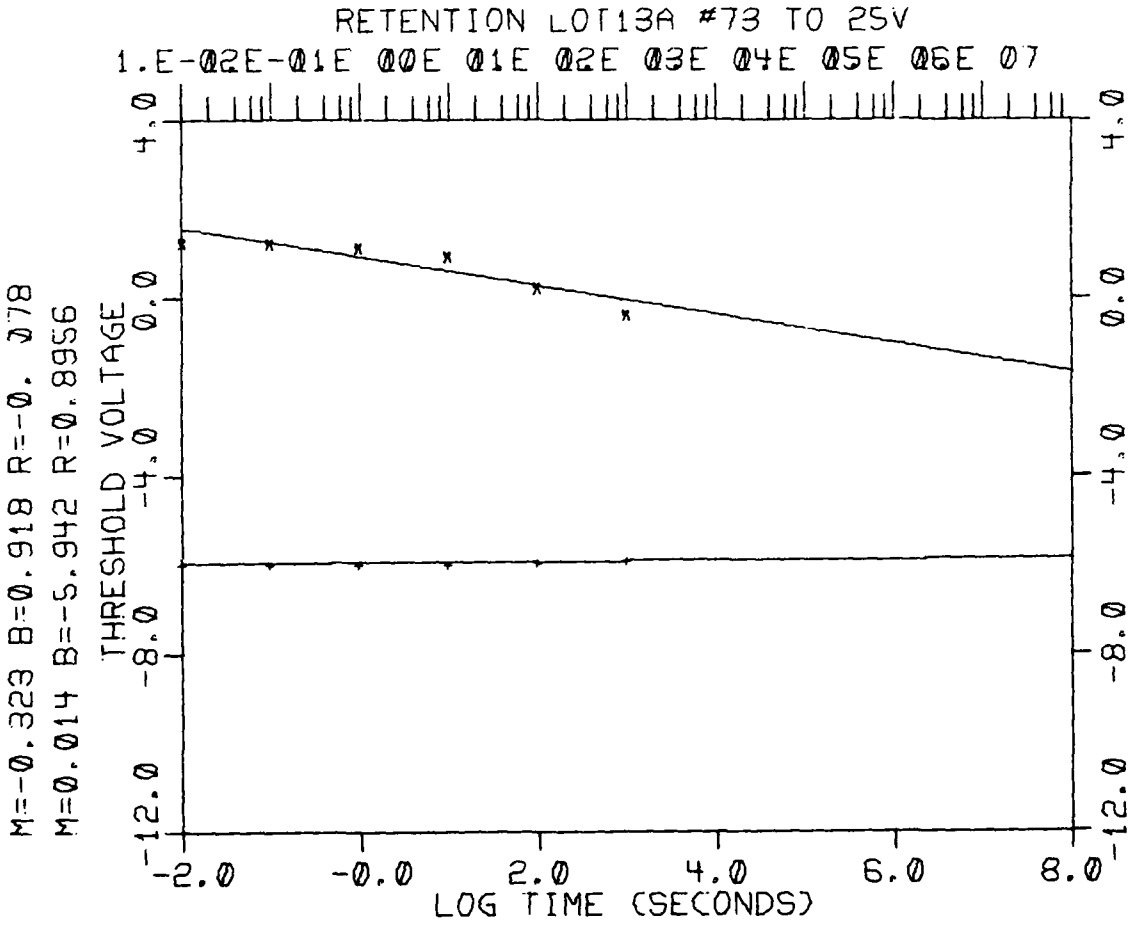

RETENTION LOT13A #73 TO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.323 B=0.918 R=-0. 978
M=0.014 B=-5.942 R=0.8956
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV- 91

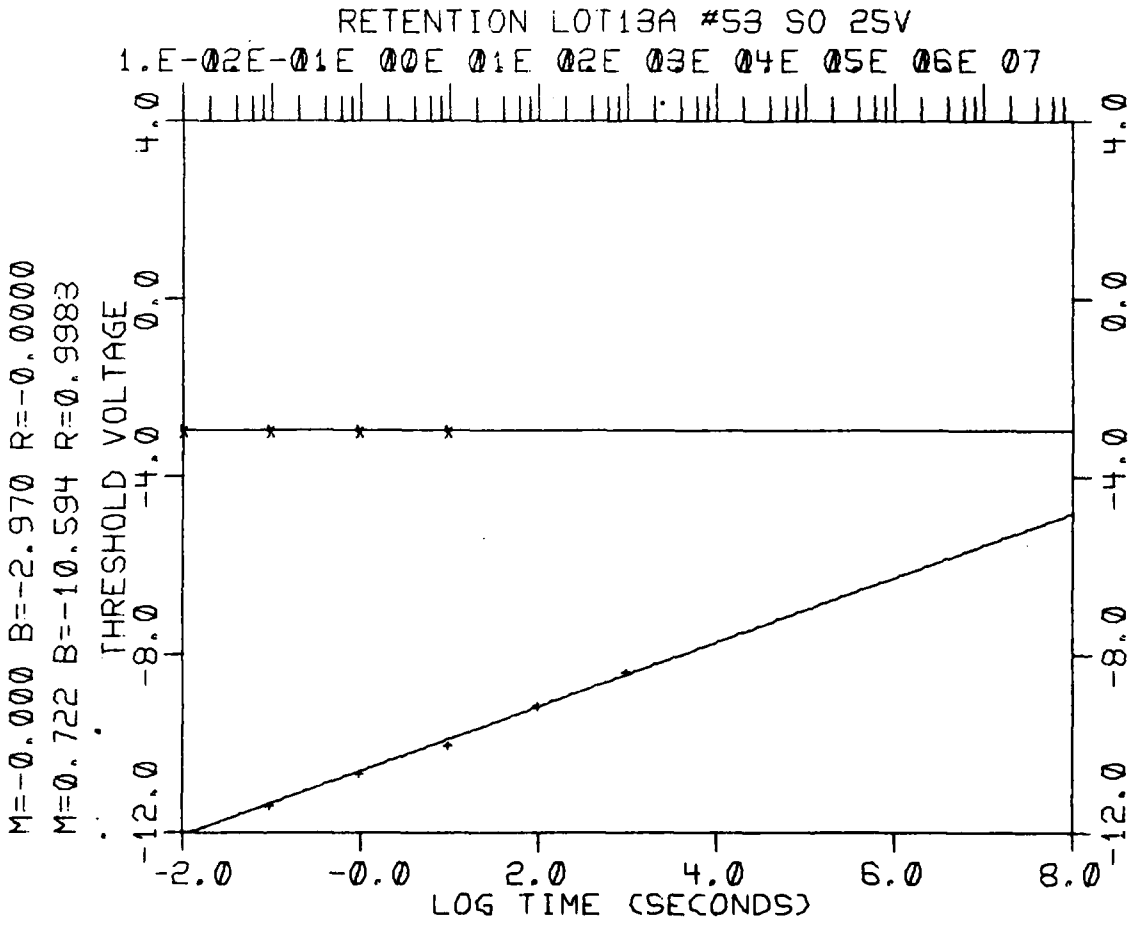

RETENTION LOT13A #53 SO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.970 R=-0.0000
M=0.722 B=-10.594 R=0.9983
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-92

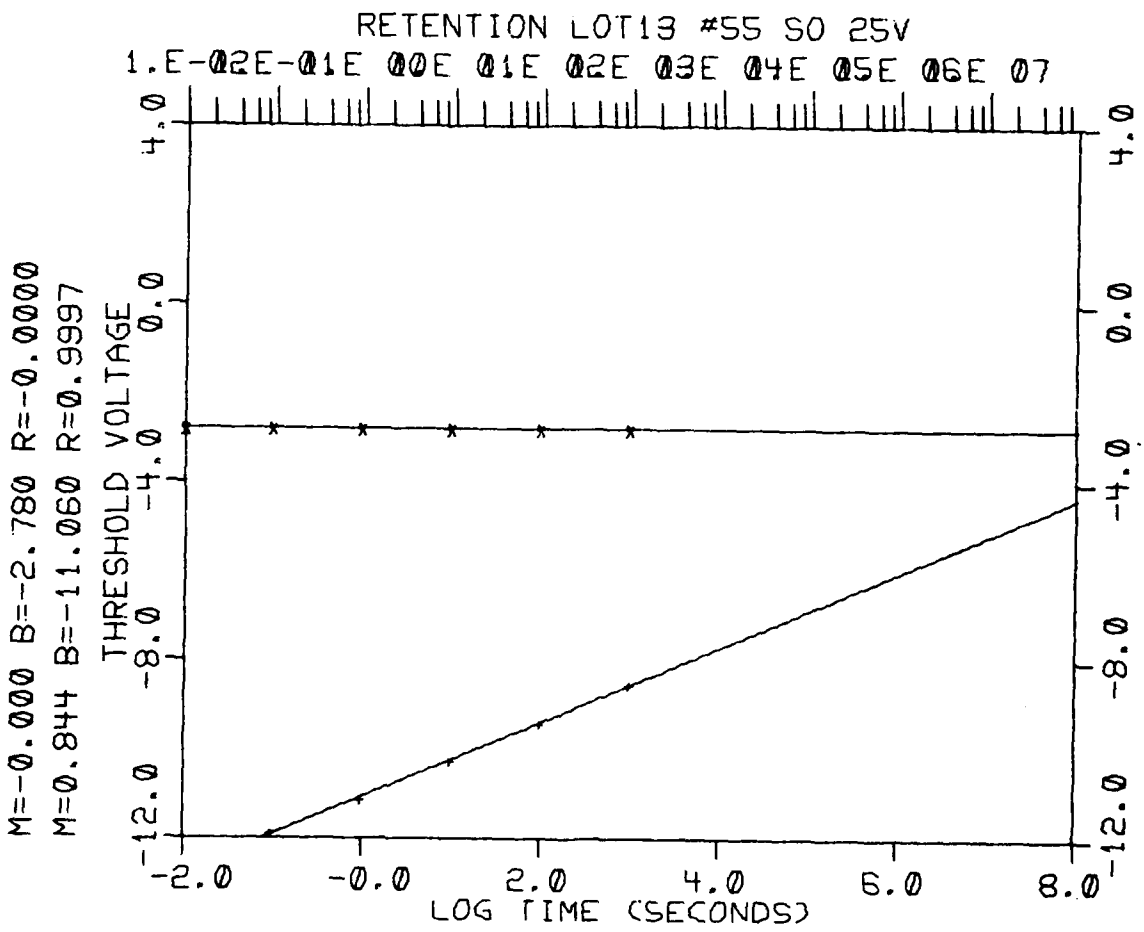

RETENTION LOT13 #55 SO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.780 R=-0.0000
M=0.844 B=-11.060 R=0.9997
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-93

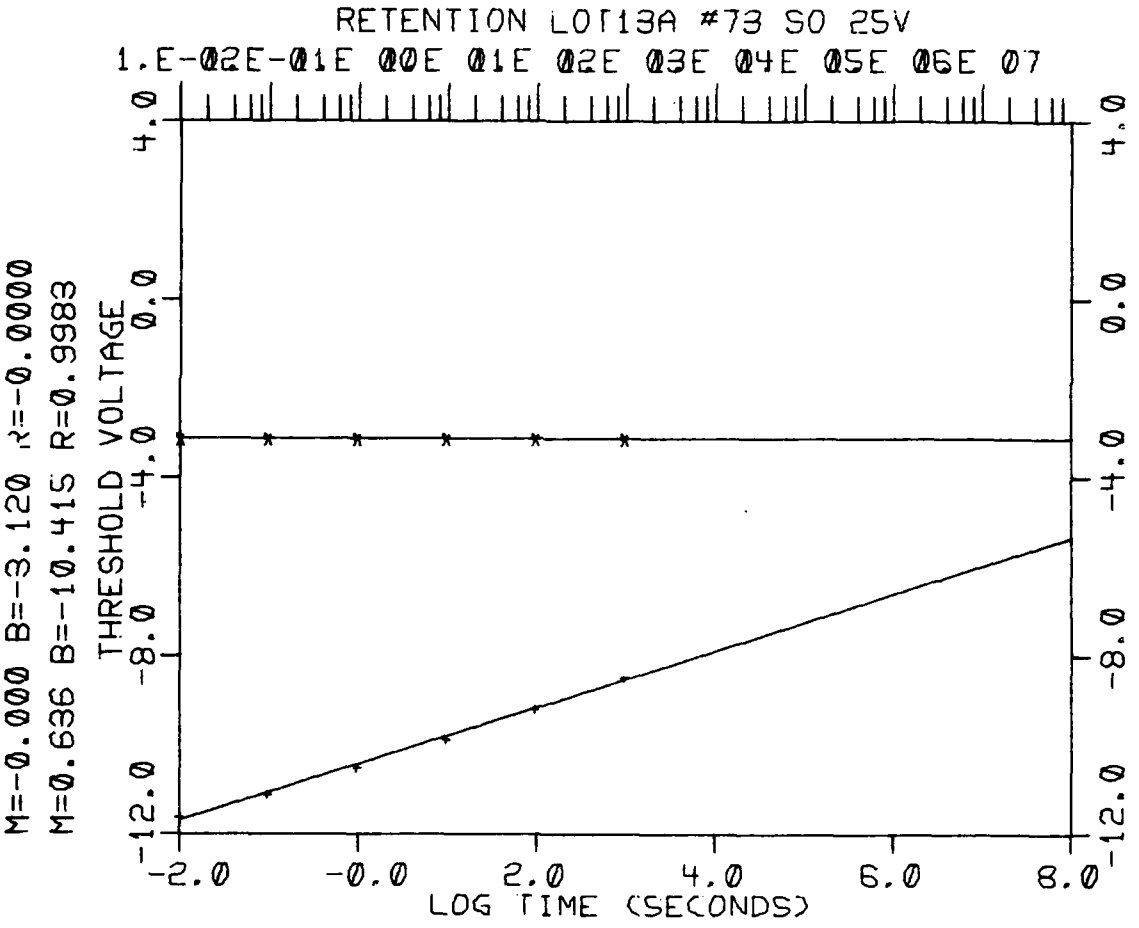

RETENTION LOT13A #73 SO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-3.120 R=-0.0000
M=0.636 B=-10.415 R=0.9983
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-94

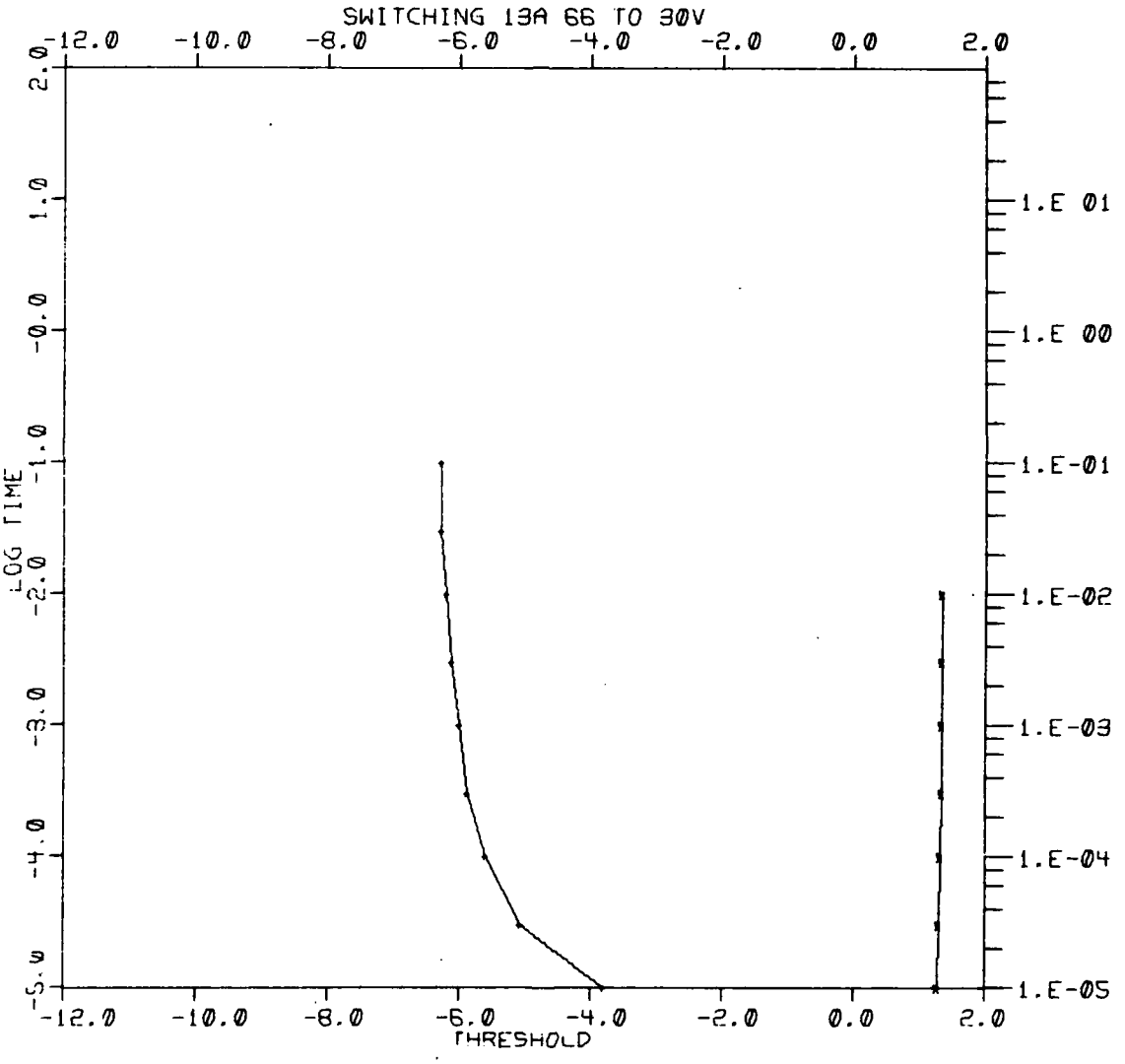

SWITCHING 13A 66 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-95

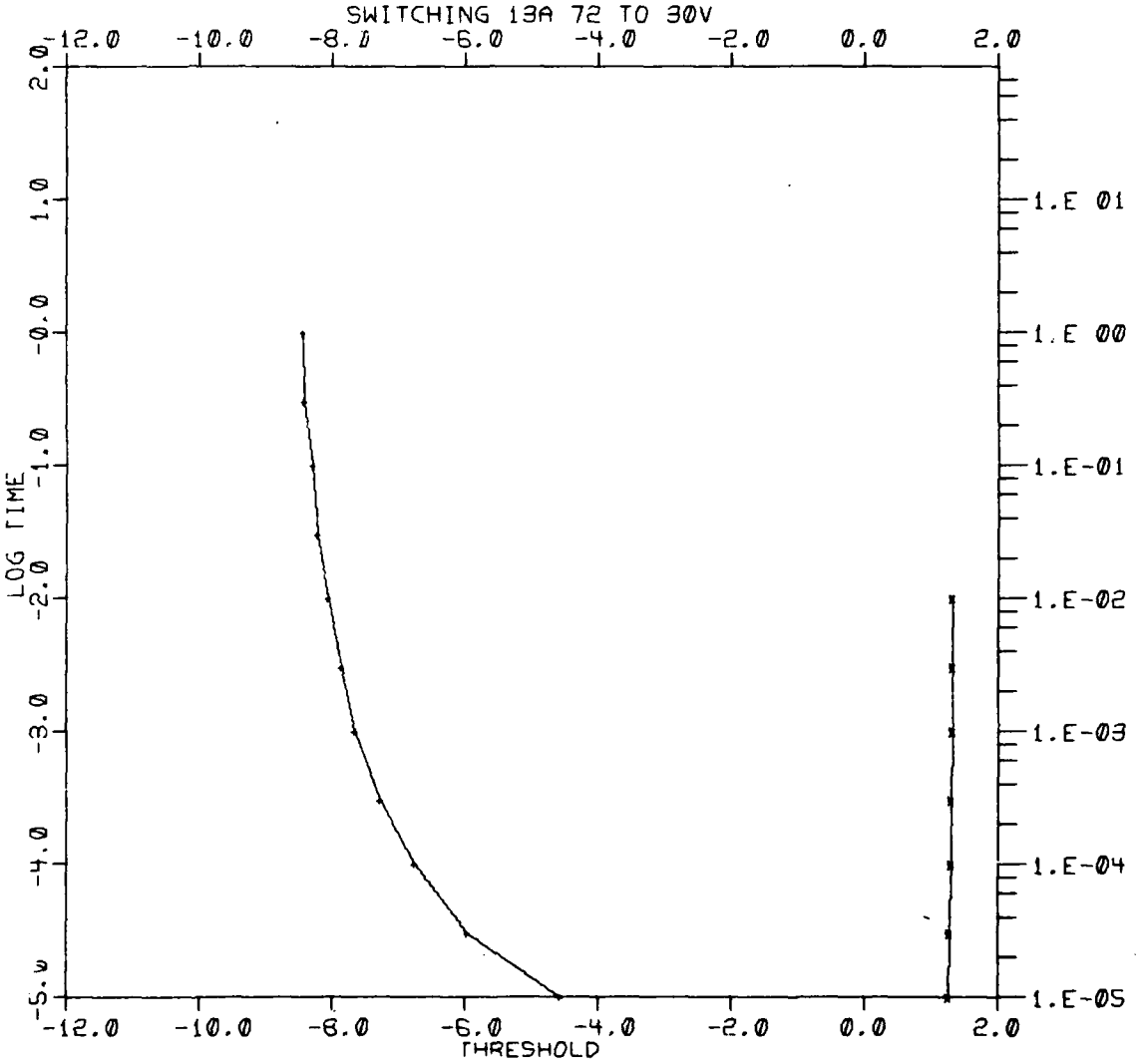

SWITCHING 13A 72 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-96

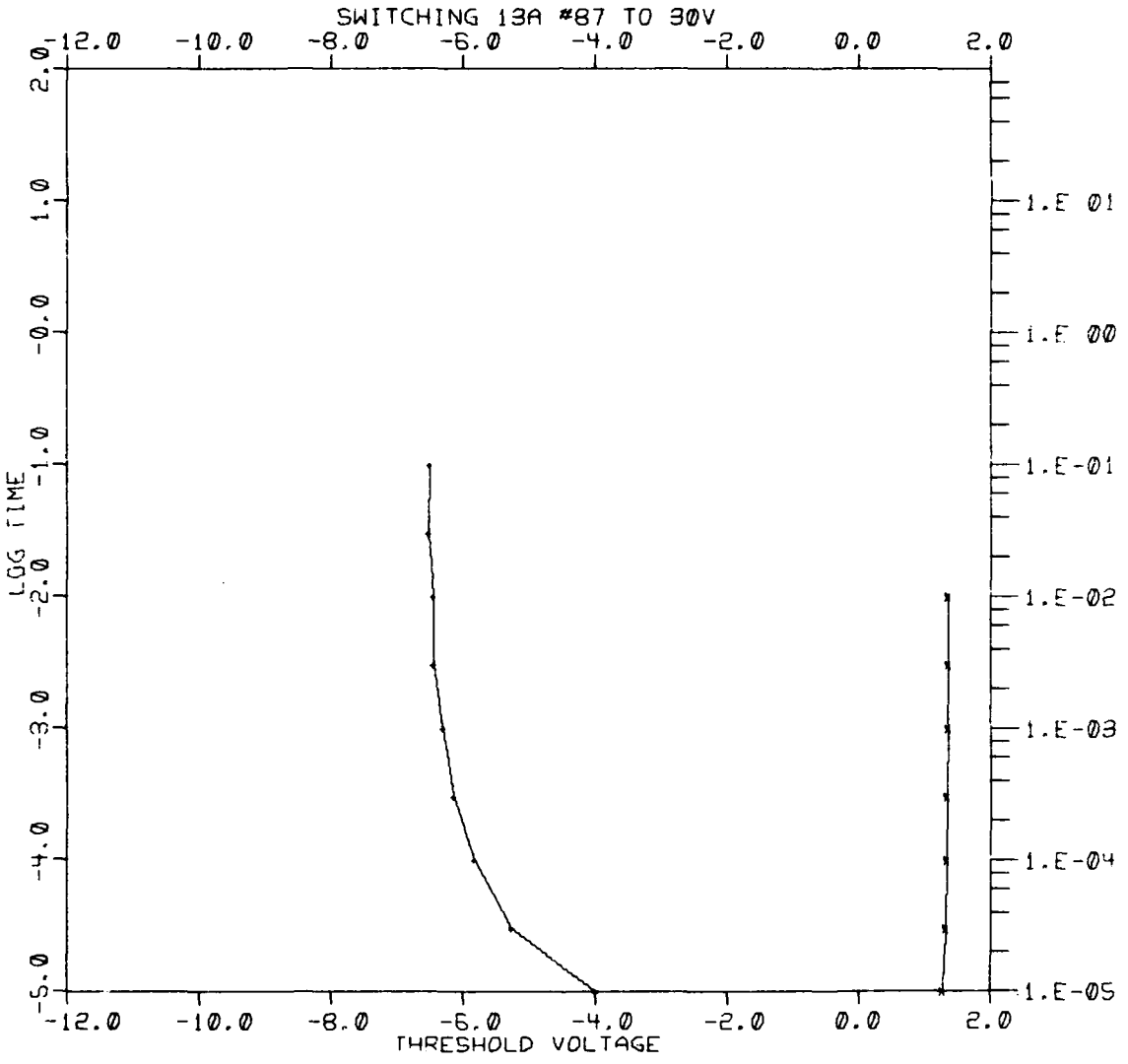

SWITCHING 13A #87 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-97

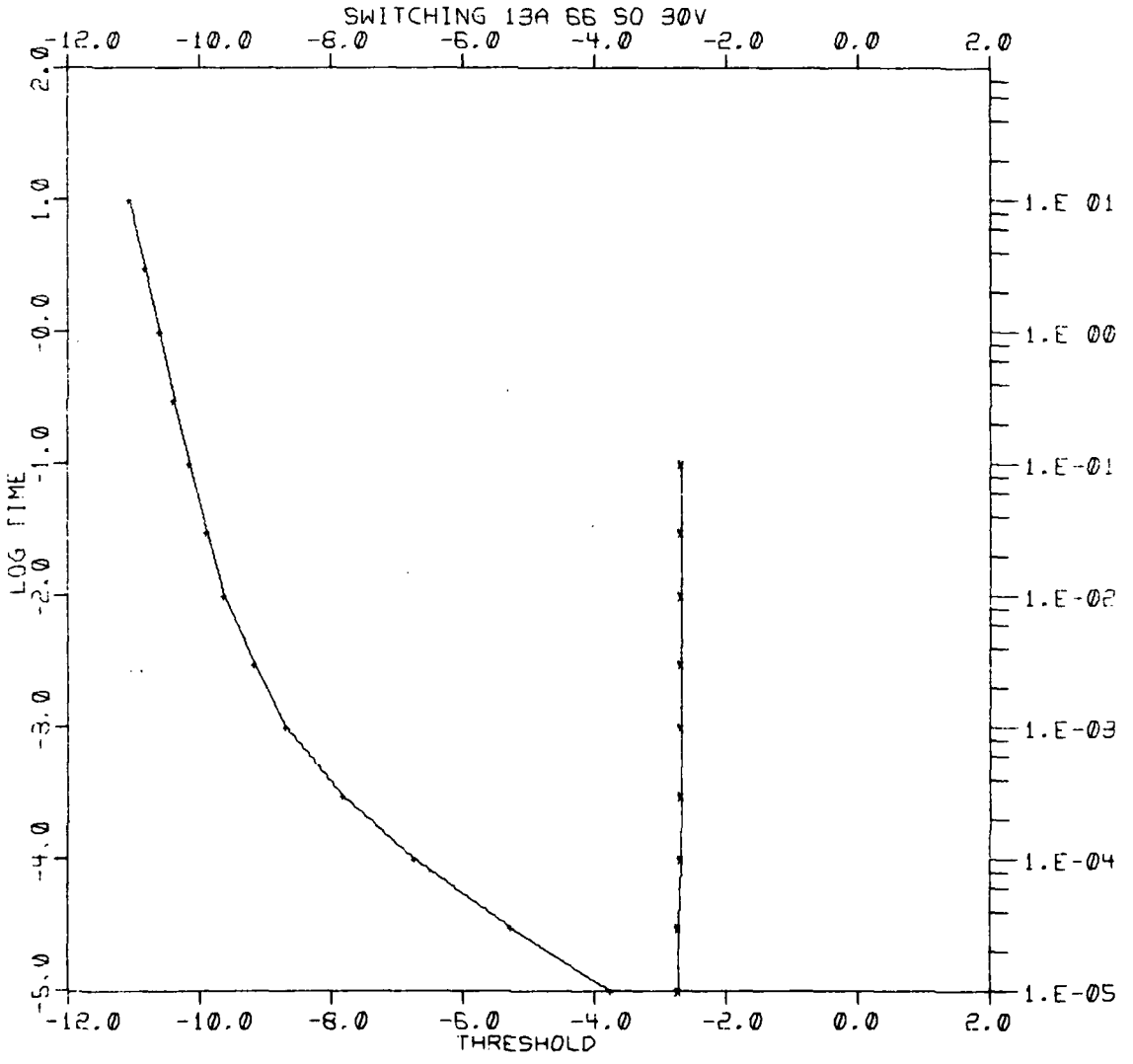

SWITCHING 13A 66 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-98

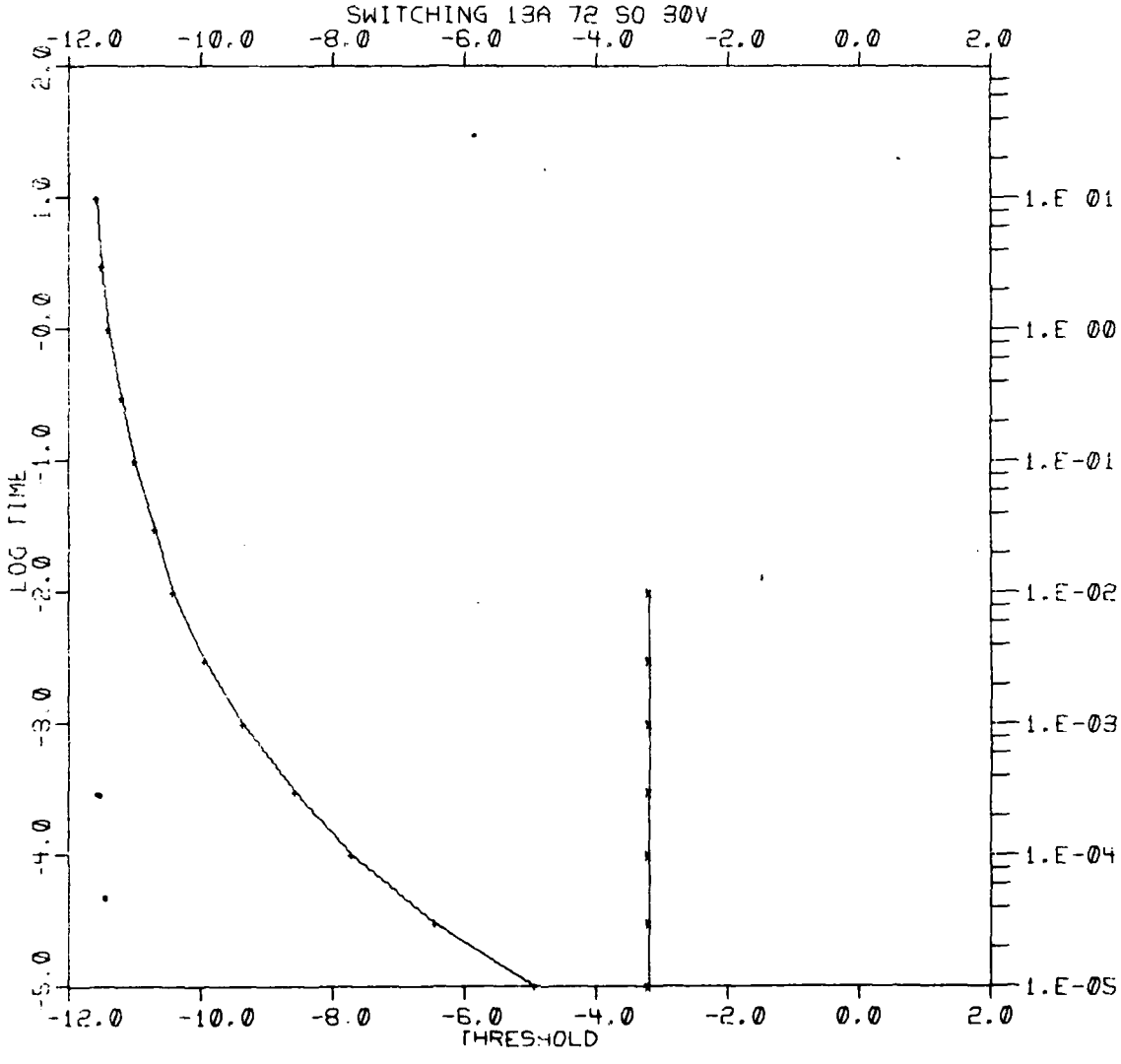

SWITCHING 13A 72 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD

Fig. IV-99

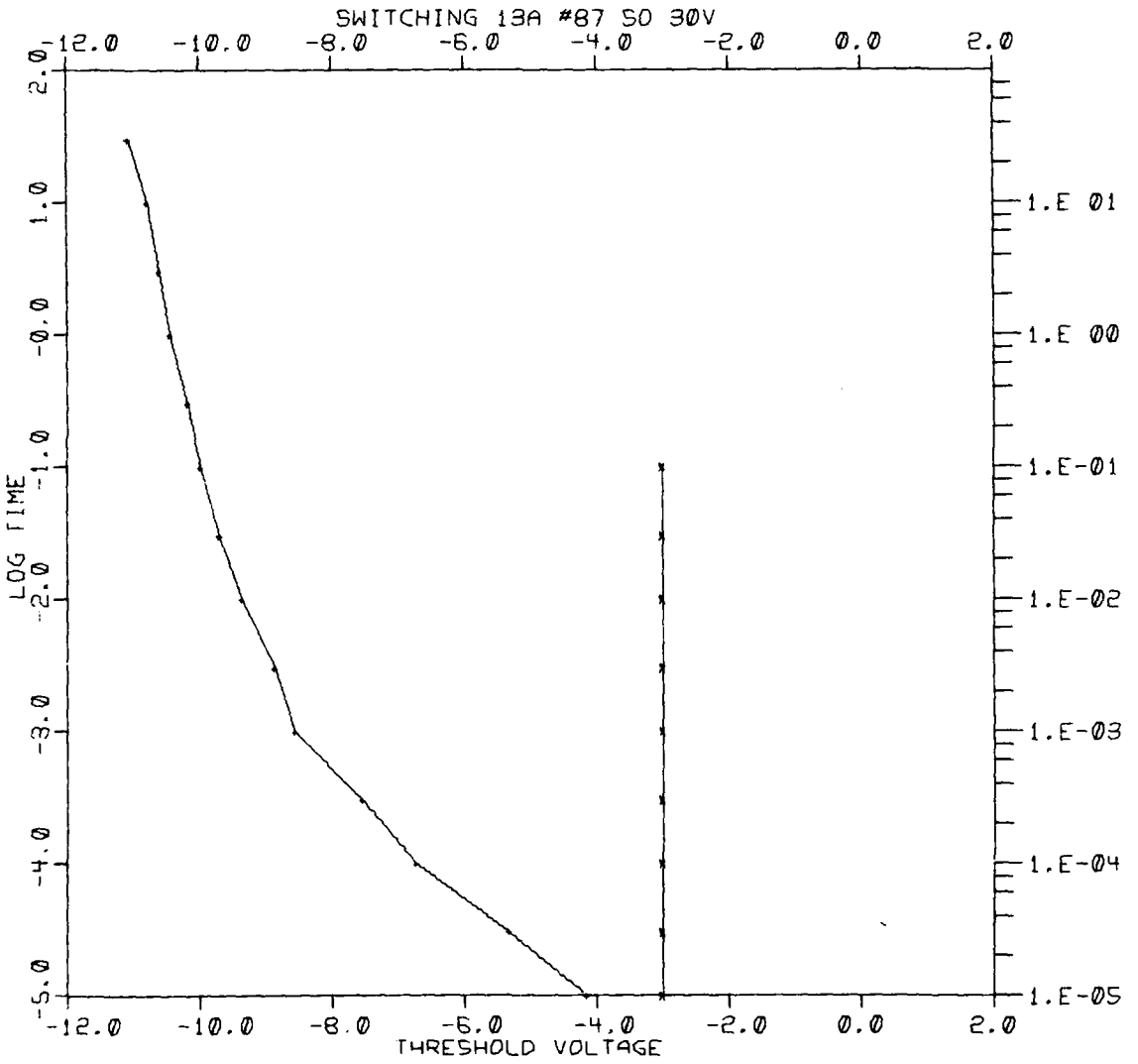

SWITCHING 13A #87 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-100

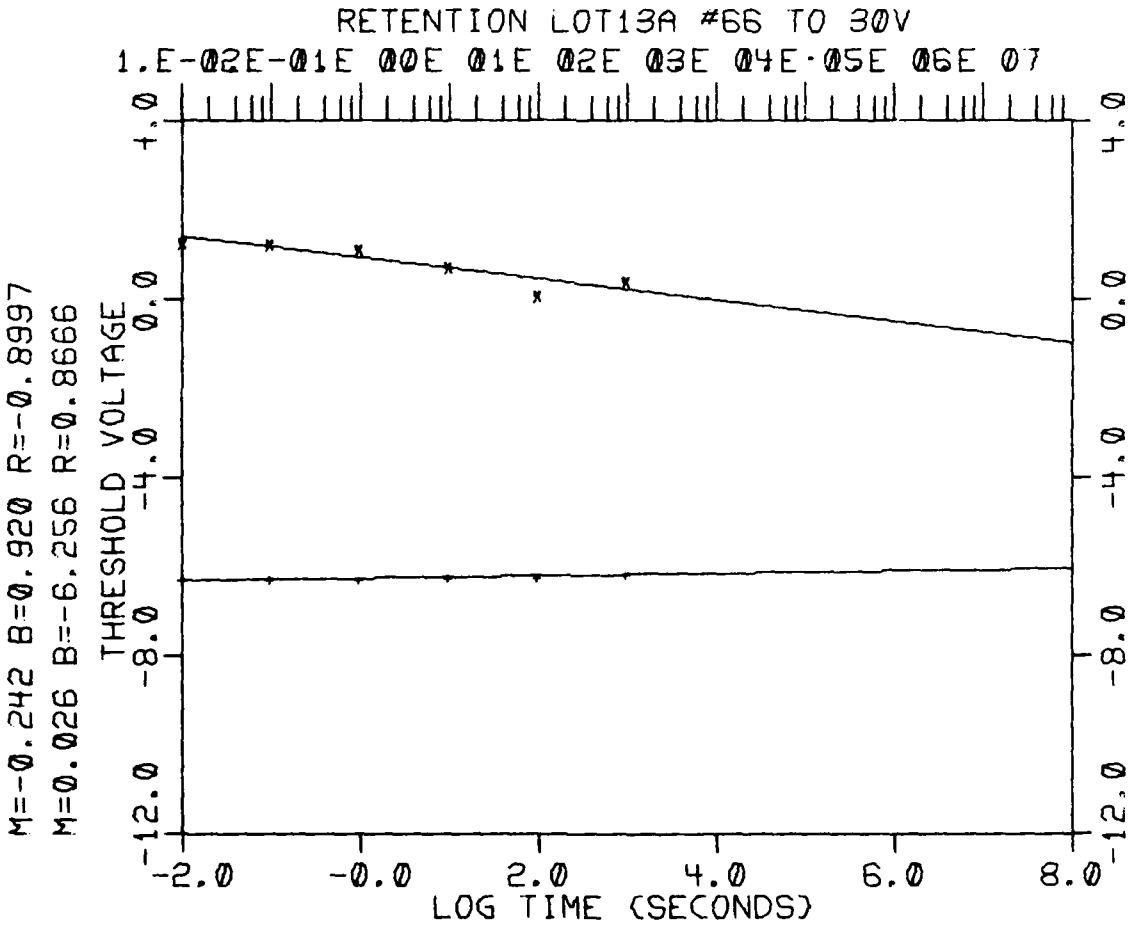

RETENTION LOT13A #66 TO 30V
1.E-02E-01E 00E 01E 02E 03E 04E·05E 06E 07
M=-0.242 B=0.920 R=-0.8997
M=0.026 B=-6.256 R=0.8666
THRESHOLD VOLTAGE
+4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-101

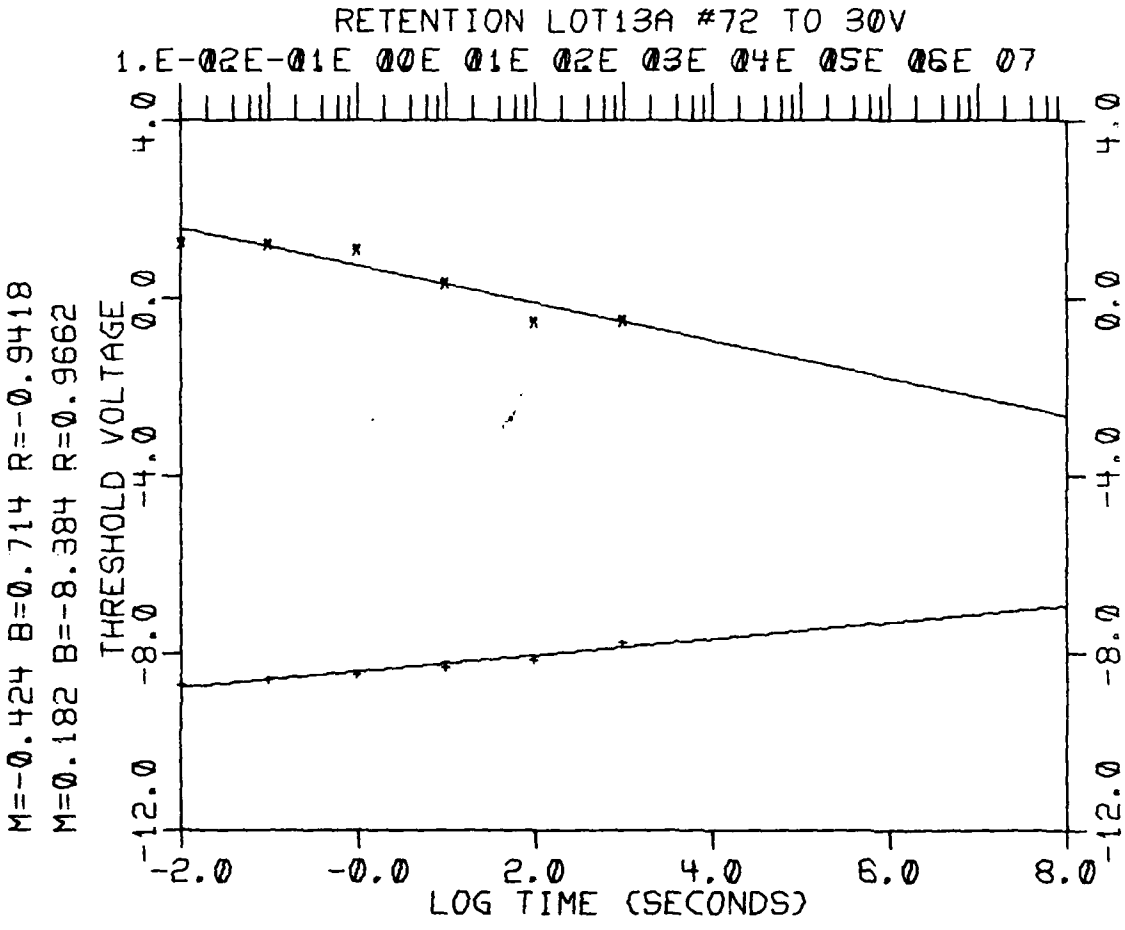

RETENTION LOT13A #72 TO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.424 B=0.714 R=-0.9418
M=0.182 B=-8.384 R=0.9662
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-102

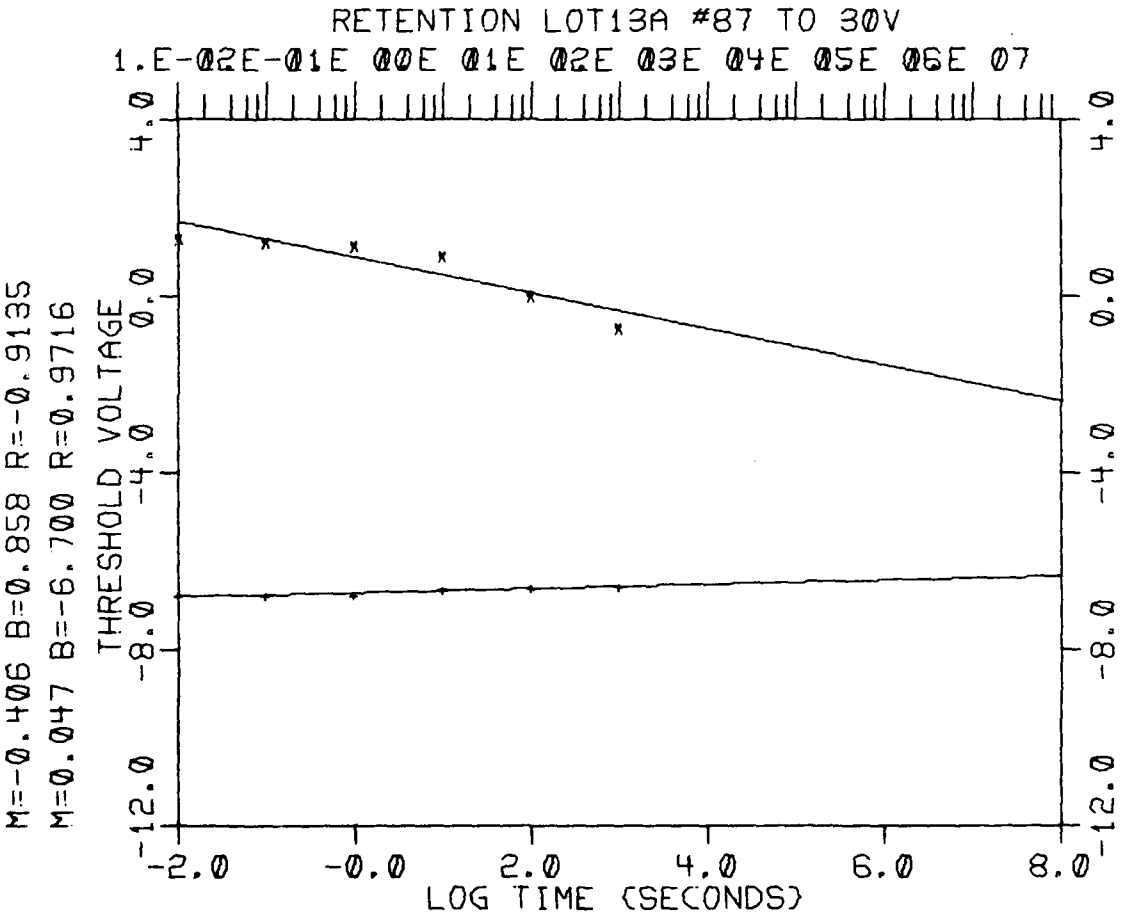

RETENTION LOT13A #87 TO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.406 B=0.858 R=-0.9135
M=0.047 B=-6.700 R=0.9716
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-103

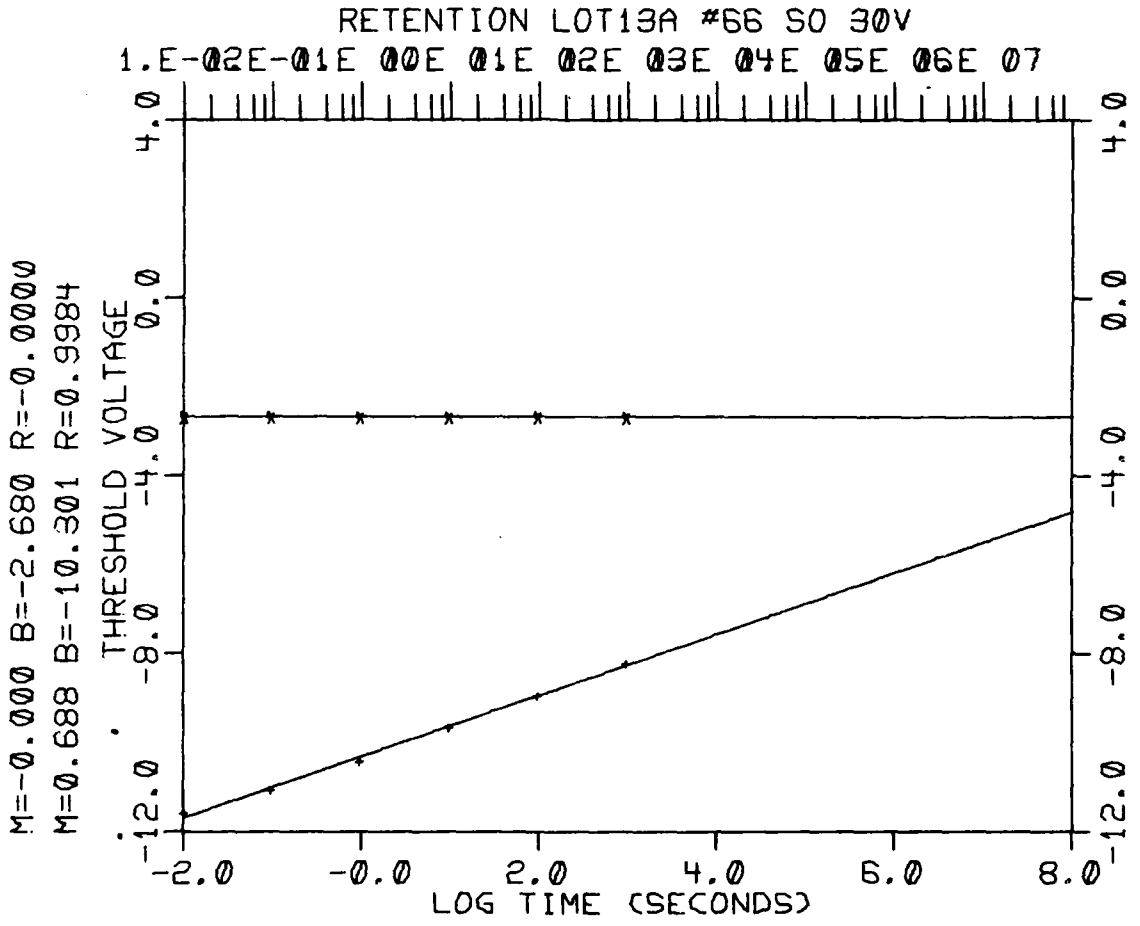

RETENTION LOT13A #66 SO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.680 R=-0.0000
M=0.688 B=-10.301 R=0.9984
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-104

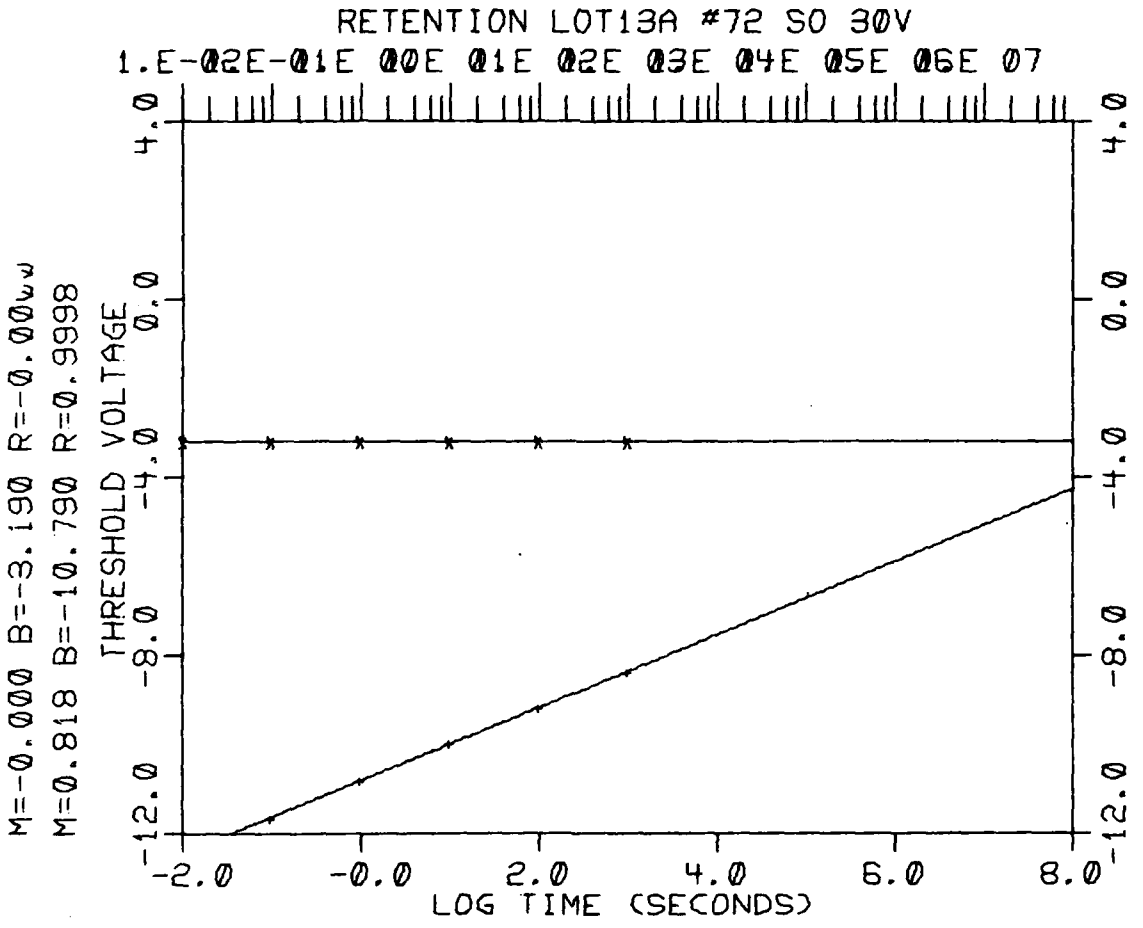

RETENTION LOT13A #72 SO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-3.190 R=-0.0000
M=0.818 B=-10.790 R=0.9998
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-105

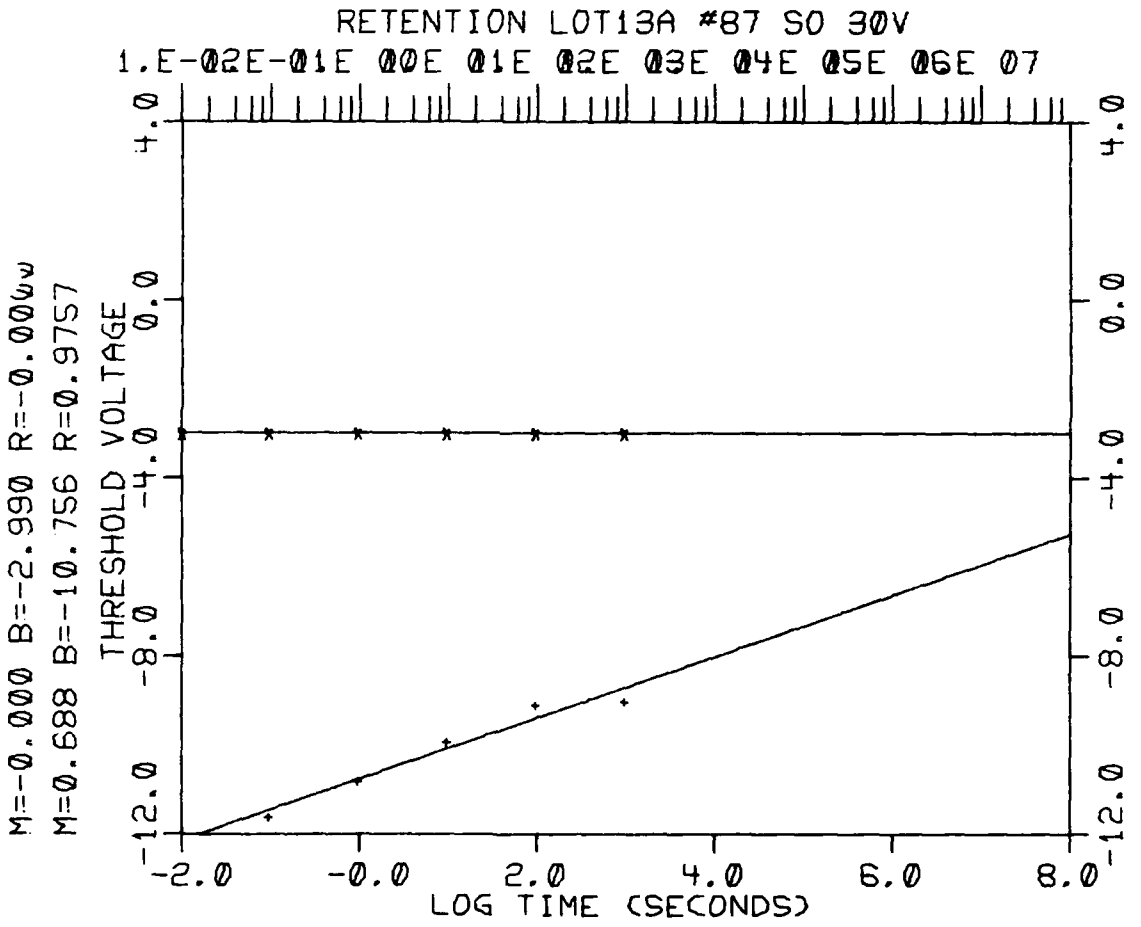

RETENTION LOT13A #87 SO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.990 R=-0.000
M=0.688 B=-10.756 R=0.9757
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-106

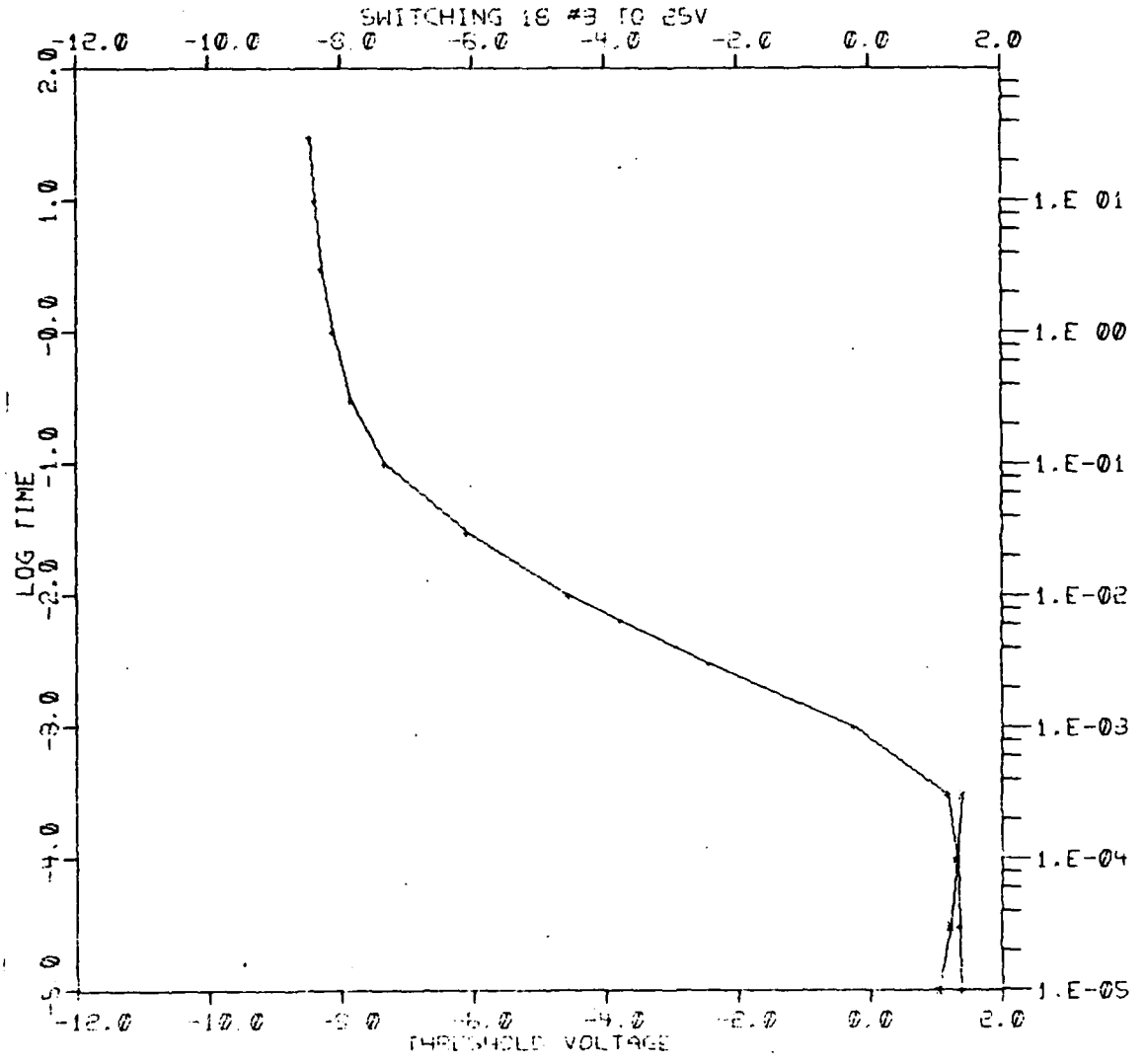

SWITCHING 18 #3 TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-107

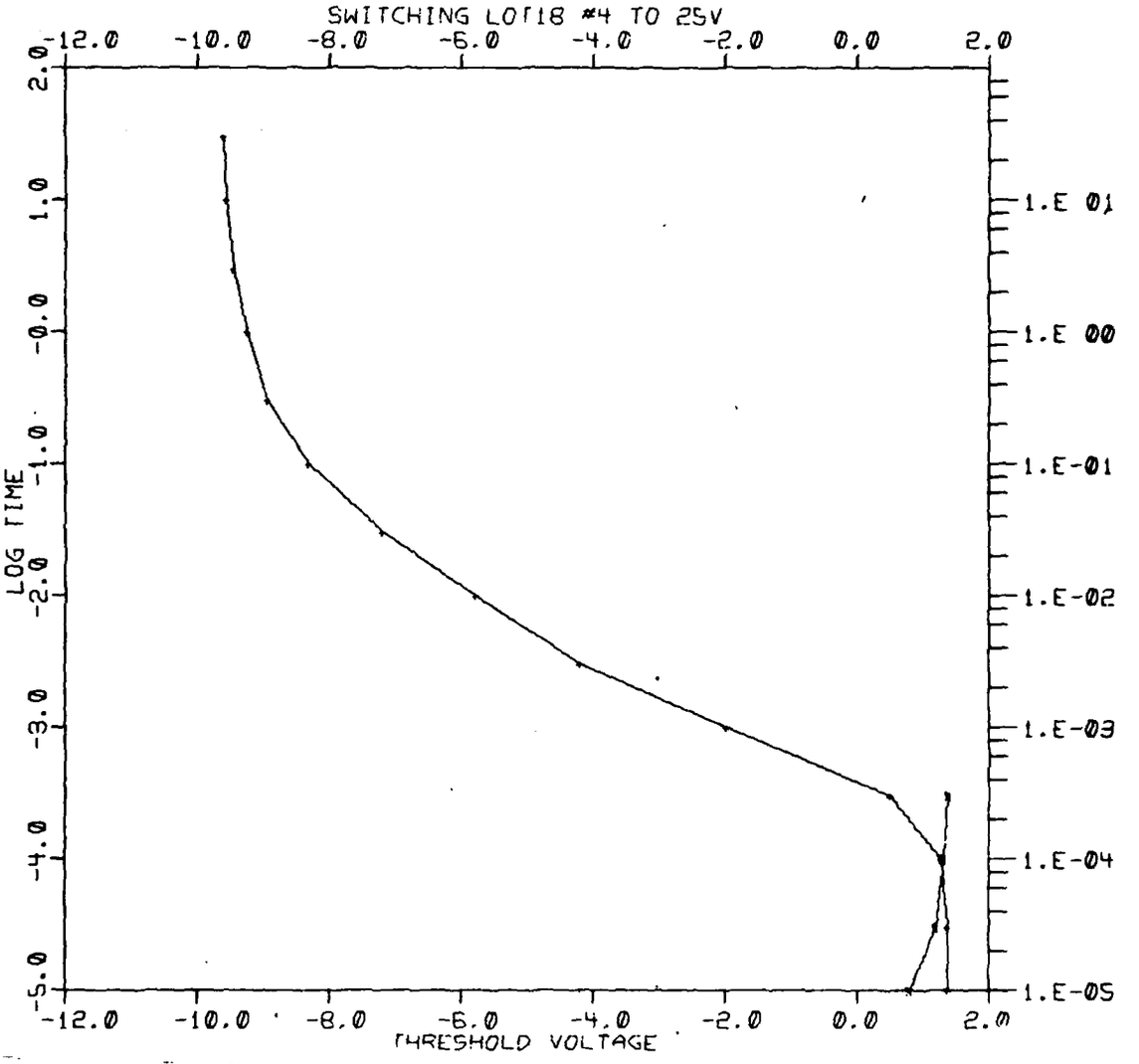

SWITCHING LOT18 #4 TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-108

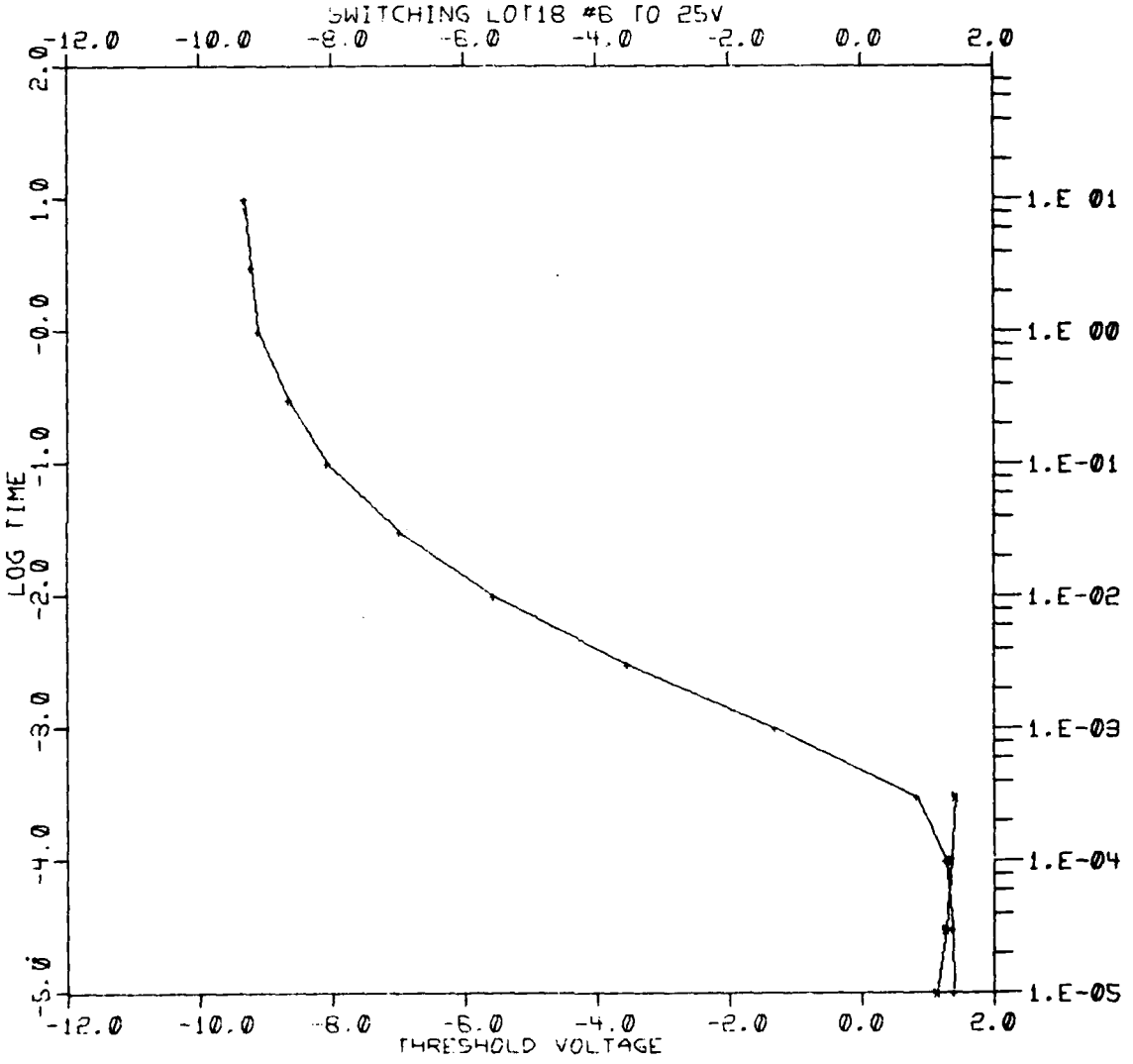

SWITCHING LOT18 #6 TO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-109

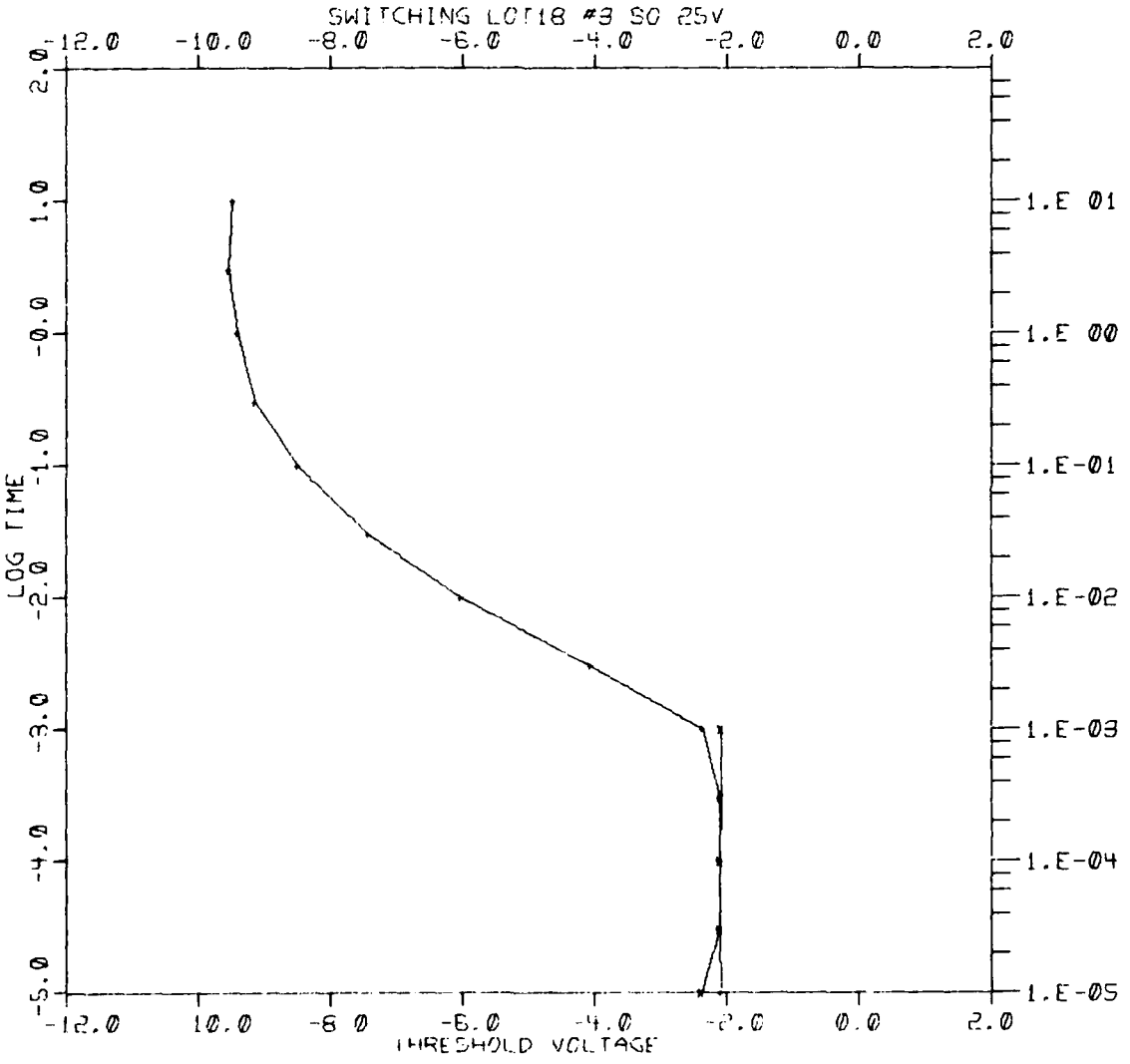

SWITCHING LOT18 #3 SO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-110

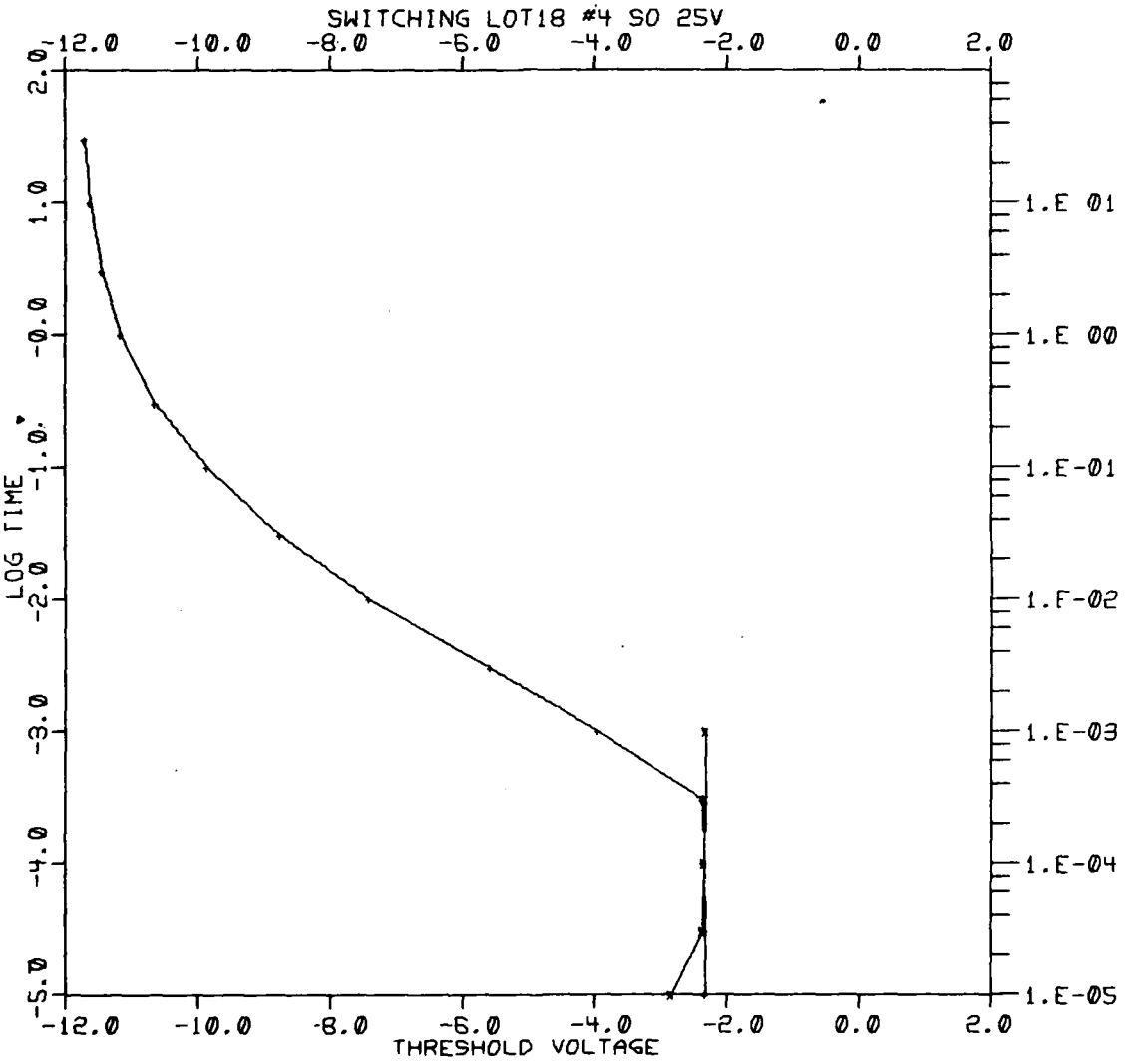

SWITCHING LOT18 #4 SO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-111

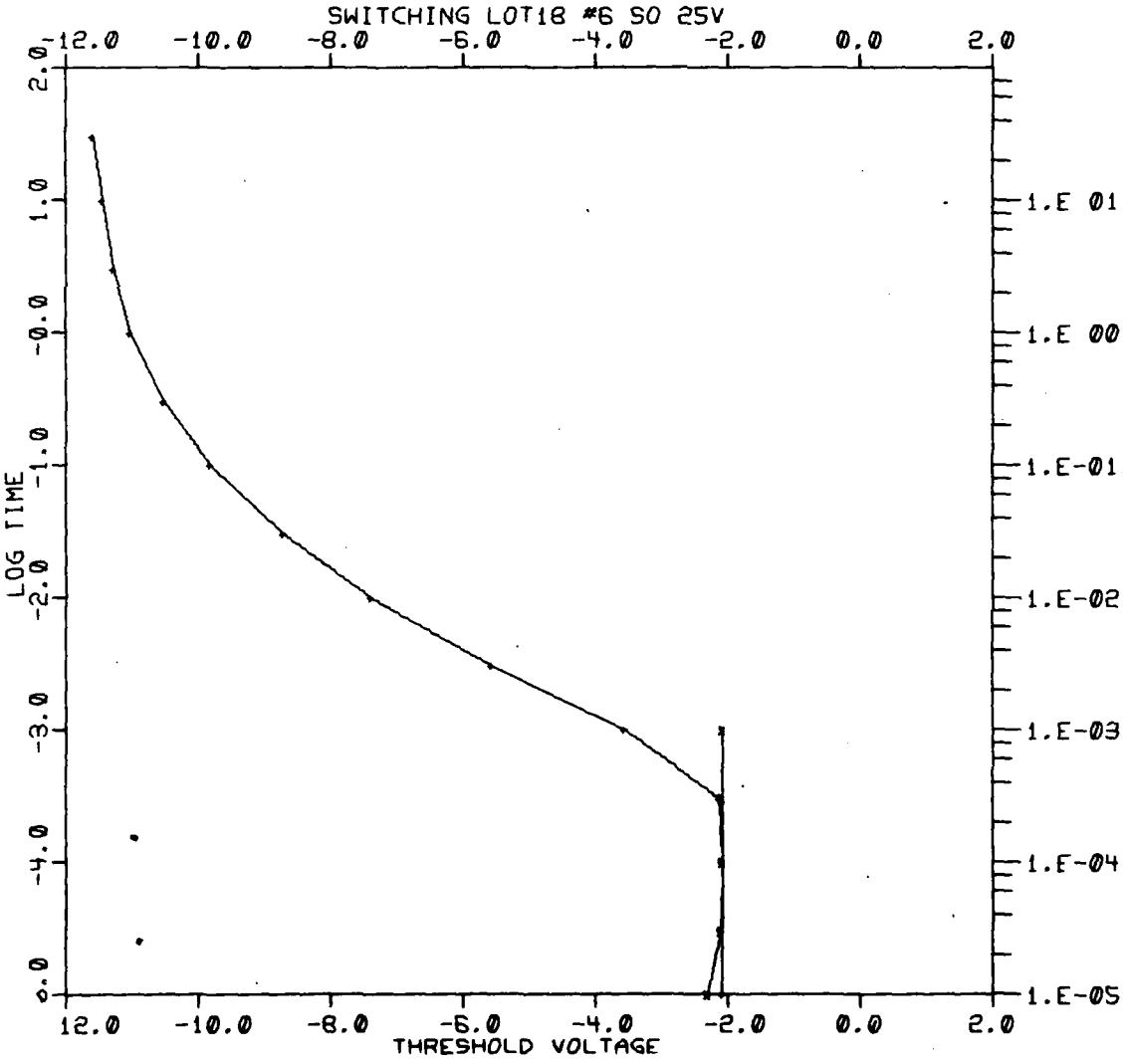

SWITCHING LOT18 #6 SO 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
LOG TIME
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
0.0
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-112

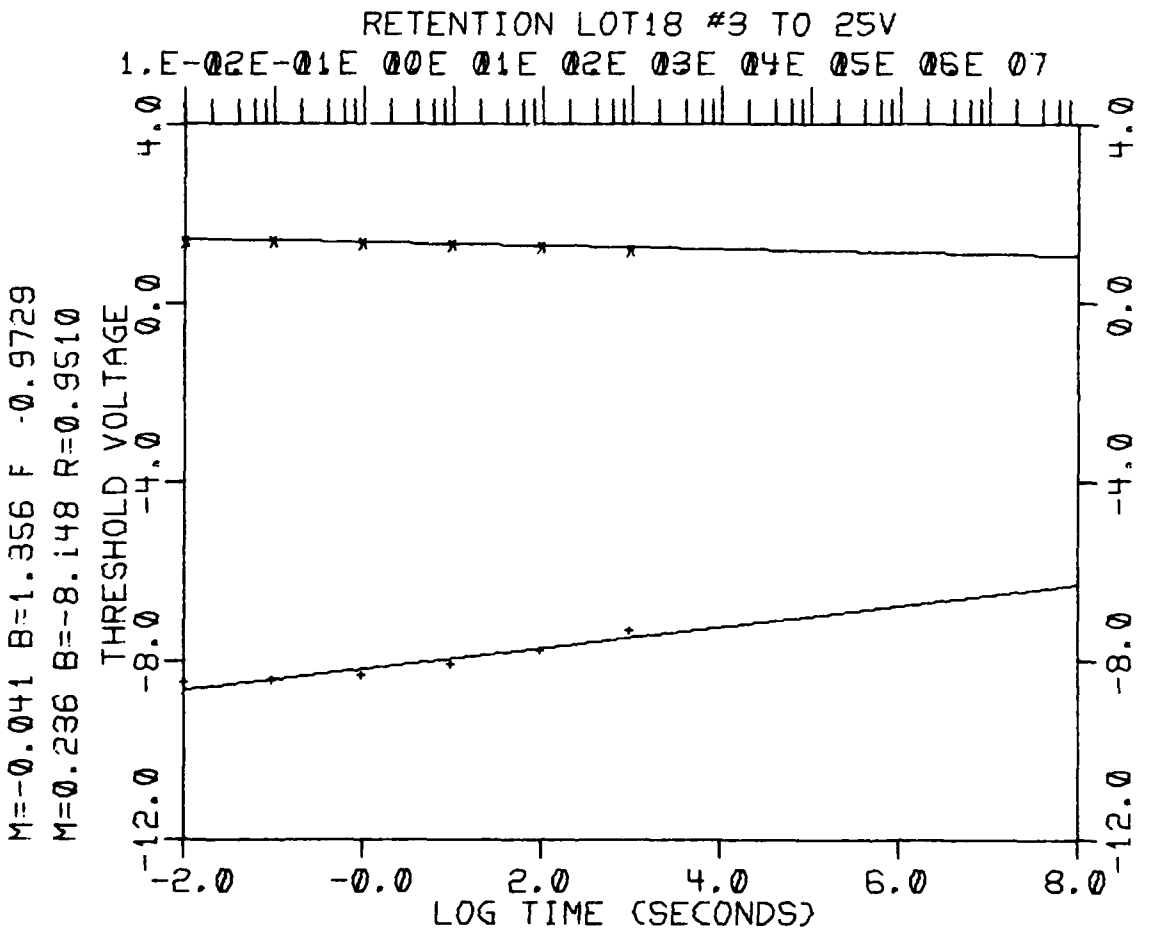

RETENTION LOT18 #3 TO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.041 B=1.356 F -0.9729
M=0.236 B=-8.148 R=0.9510
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-113

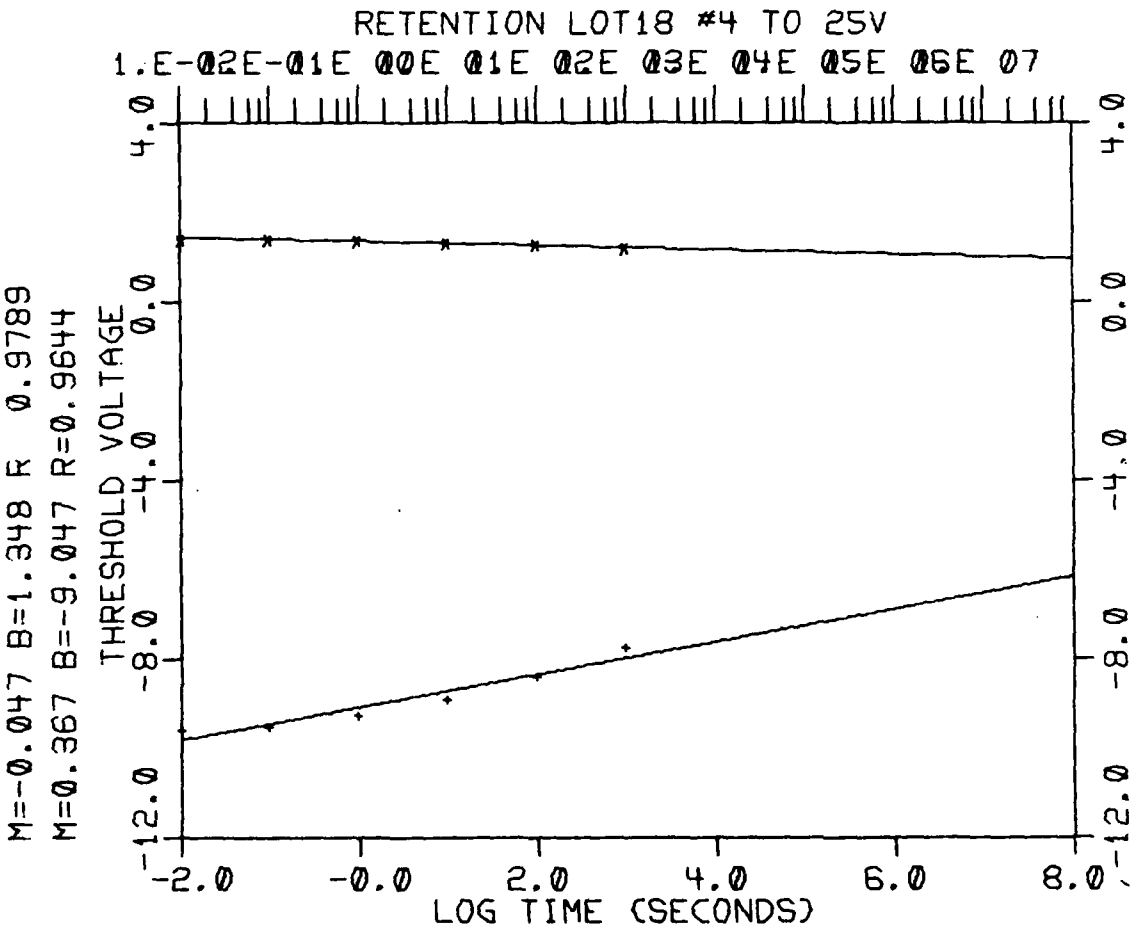

RETENTION LOT18 #4 TO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.047 B=1.348 R 0.9789
M=0.367 B=-9.047 R=0.9644
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-114

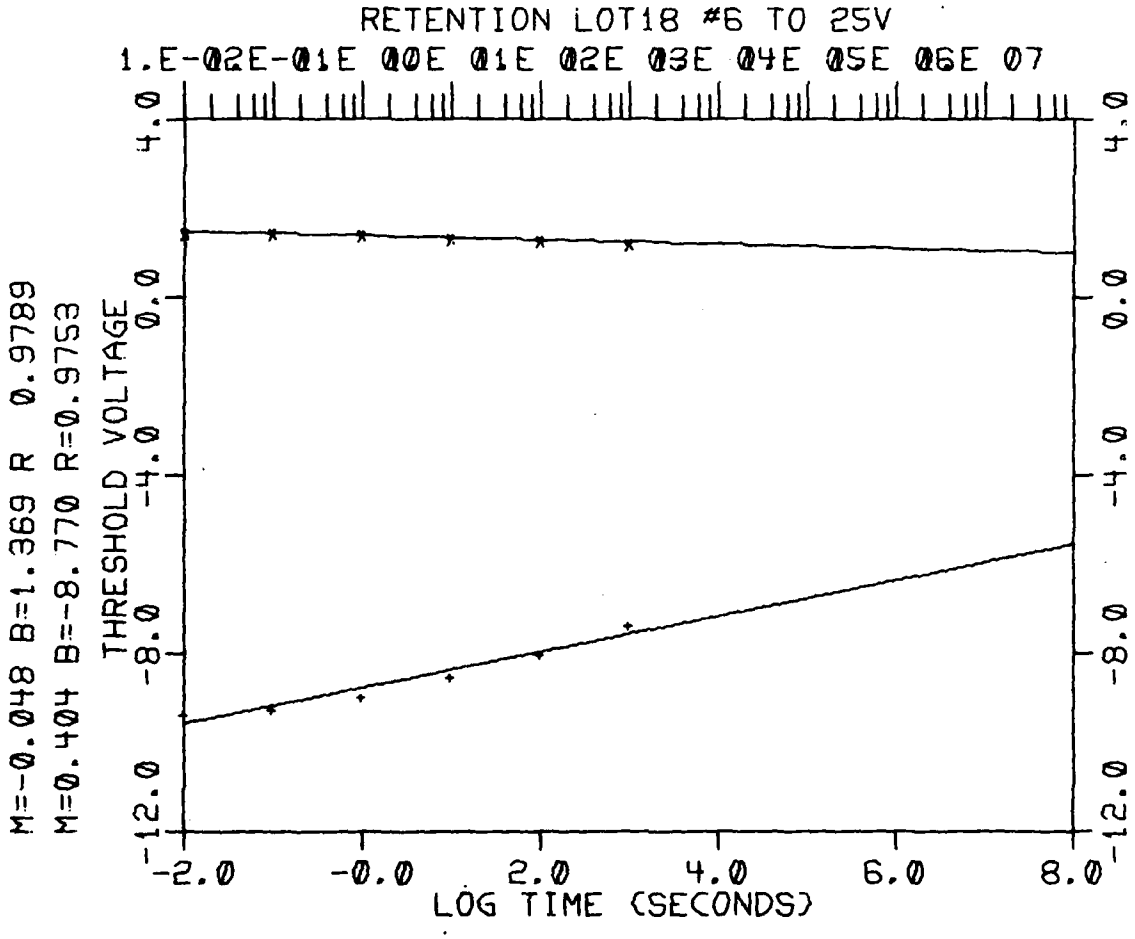

RETENTION LOT18 #6 TO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.048 B=1.369 R 0.9789
M=0.404 B=-8.770 R=0.9753
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-115

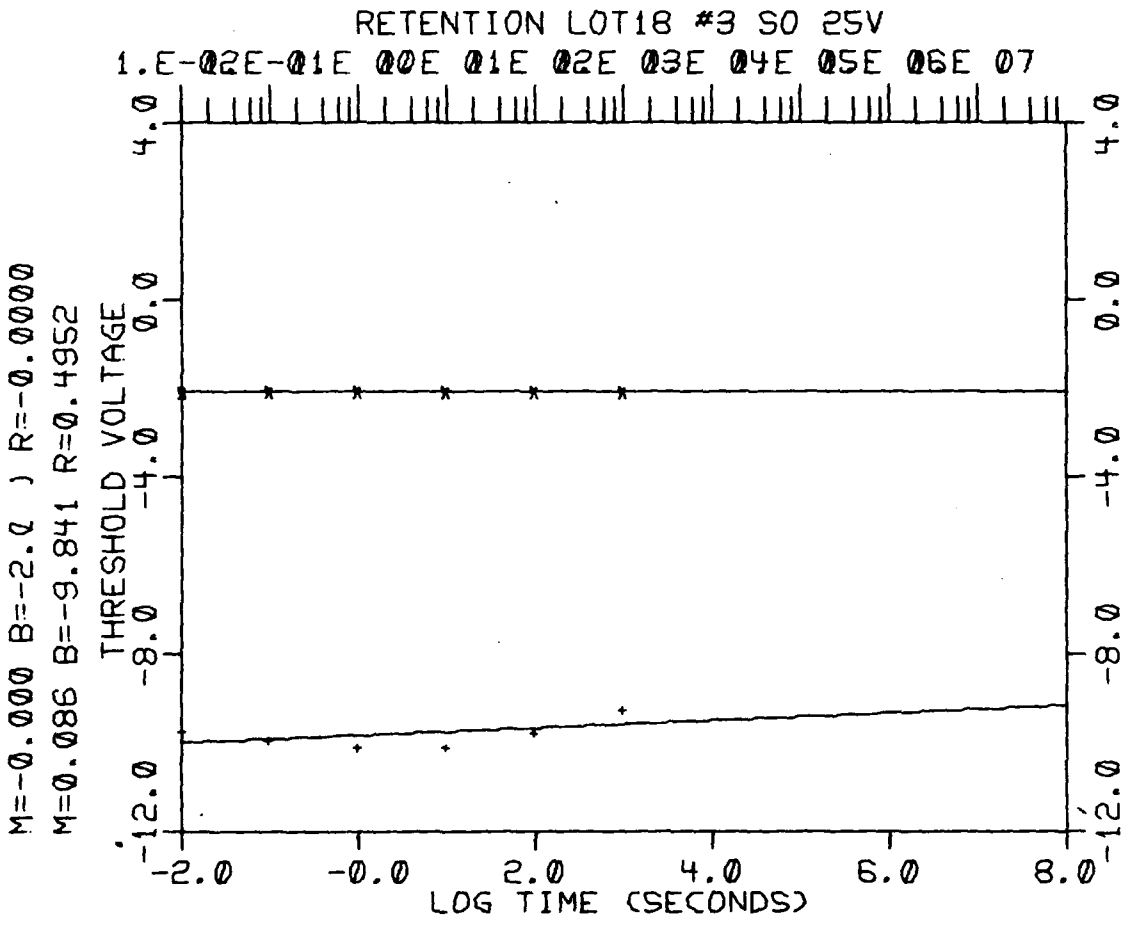

RETENTION LOT18 #3 SO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.0) R=-0.0000
M=0.086 B=-9.841 R=0.4952
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-116

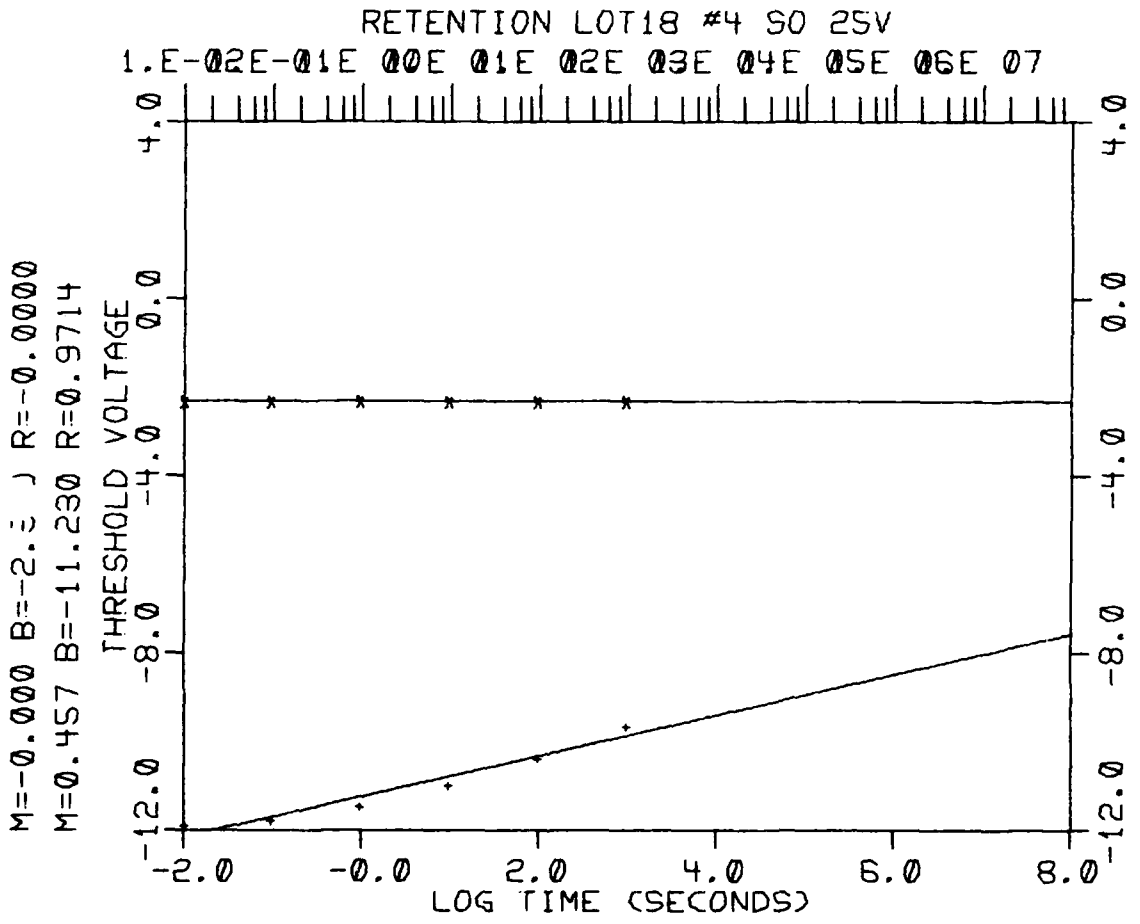

RETENTION LOT18 #4 SO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.3) R=-0.0000
M=0.457 B=-11.230 R=0.9714
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-117

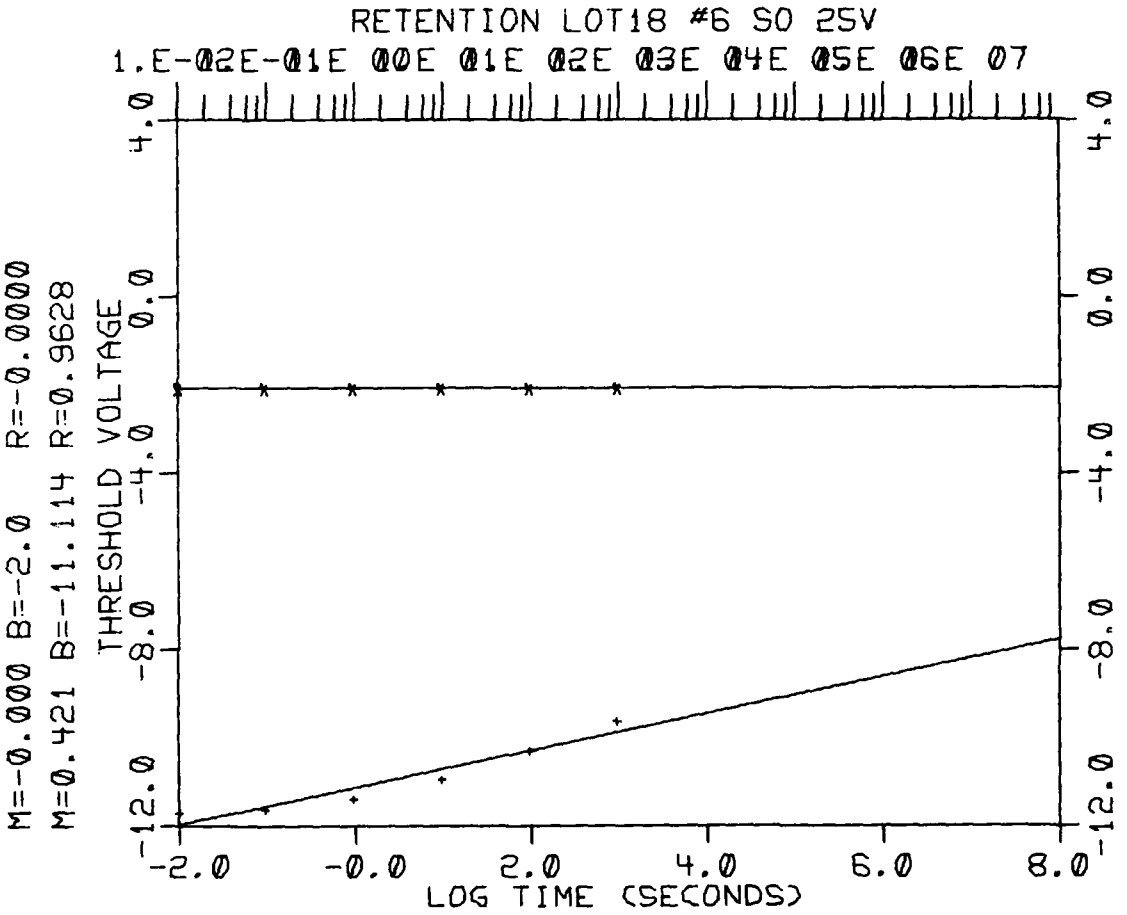

RETENTION LOT18 #6 SO 25V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.0 R=-0.0000
M=0.421 B=-11.114 R=0.9628
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-118

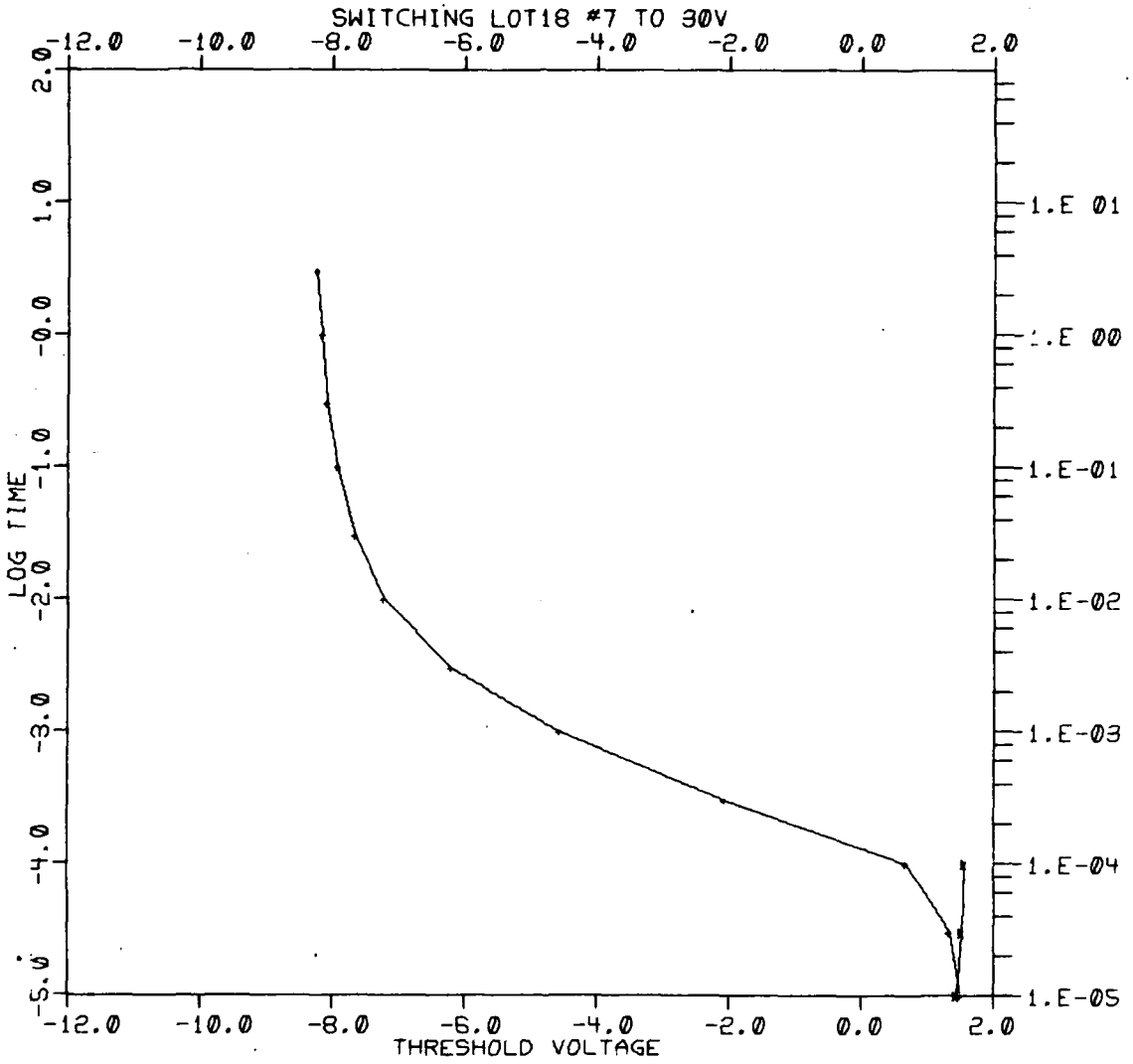

SWITCHING LOT18 #7 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-119

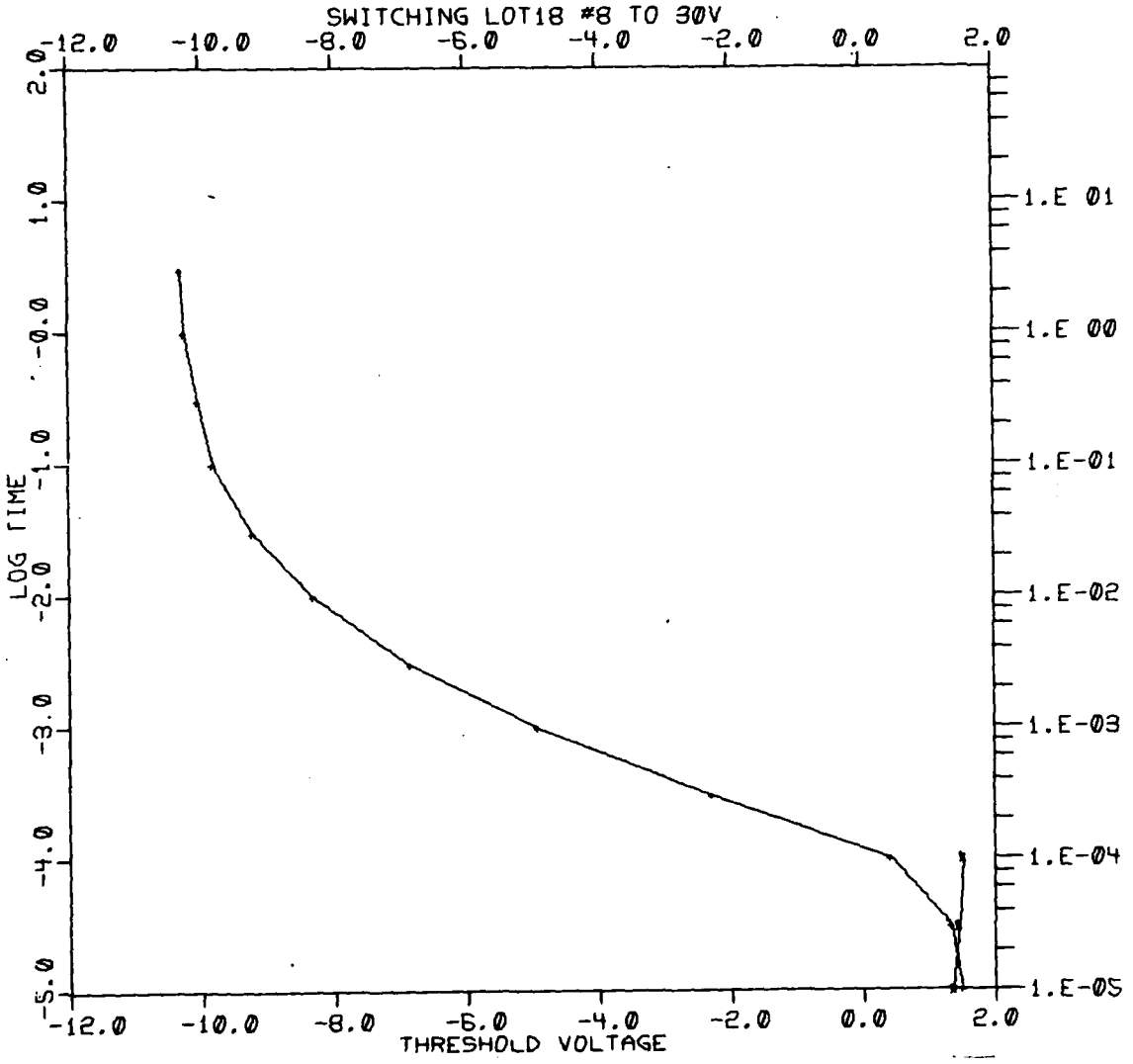

SWITCHING LOT18 #8 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-120

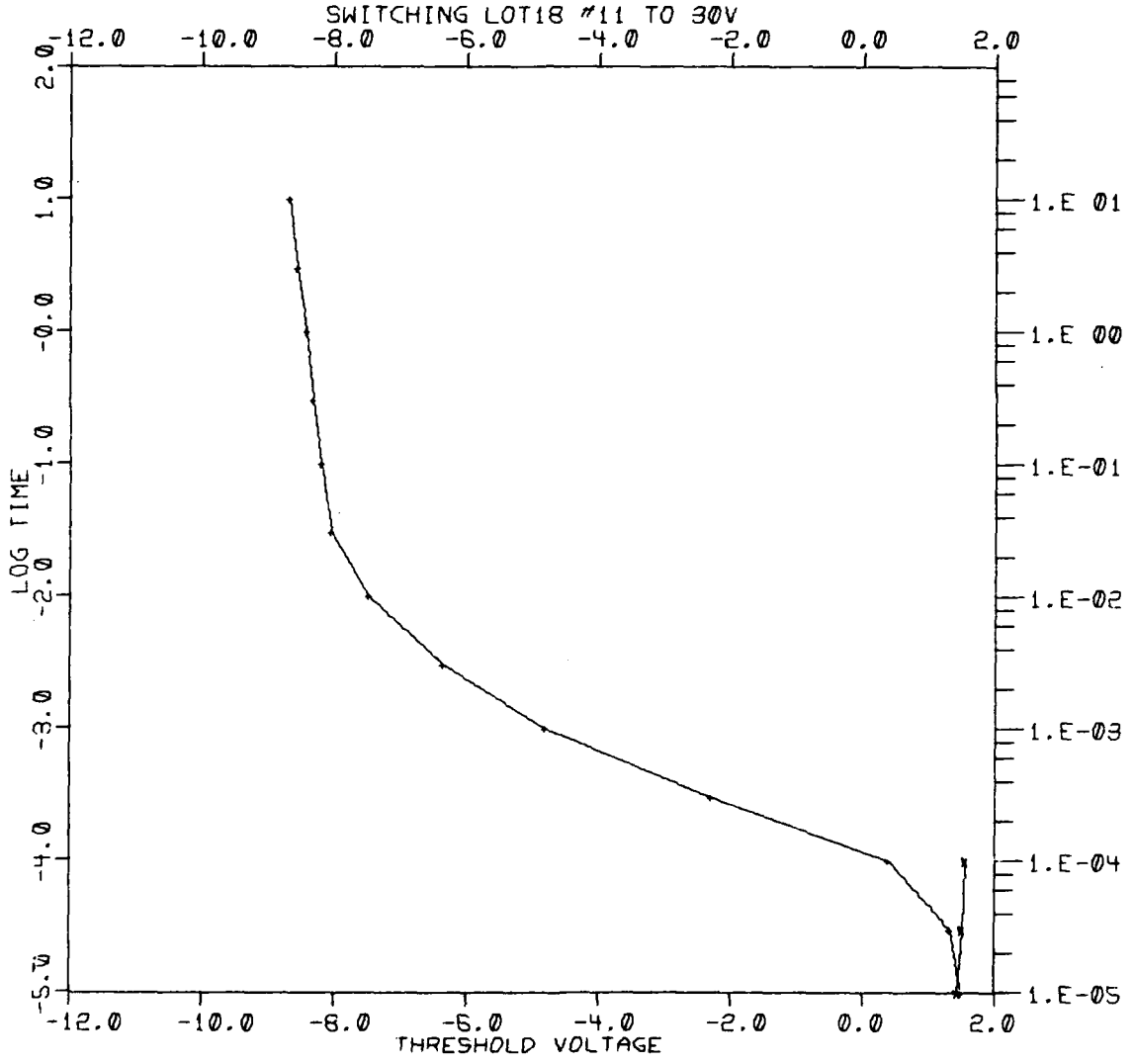

SWITCHING LOT18 #11 TO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-121

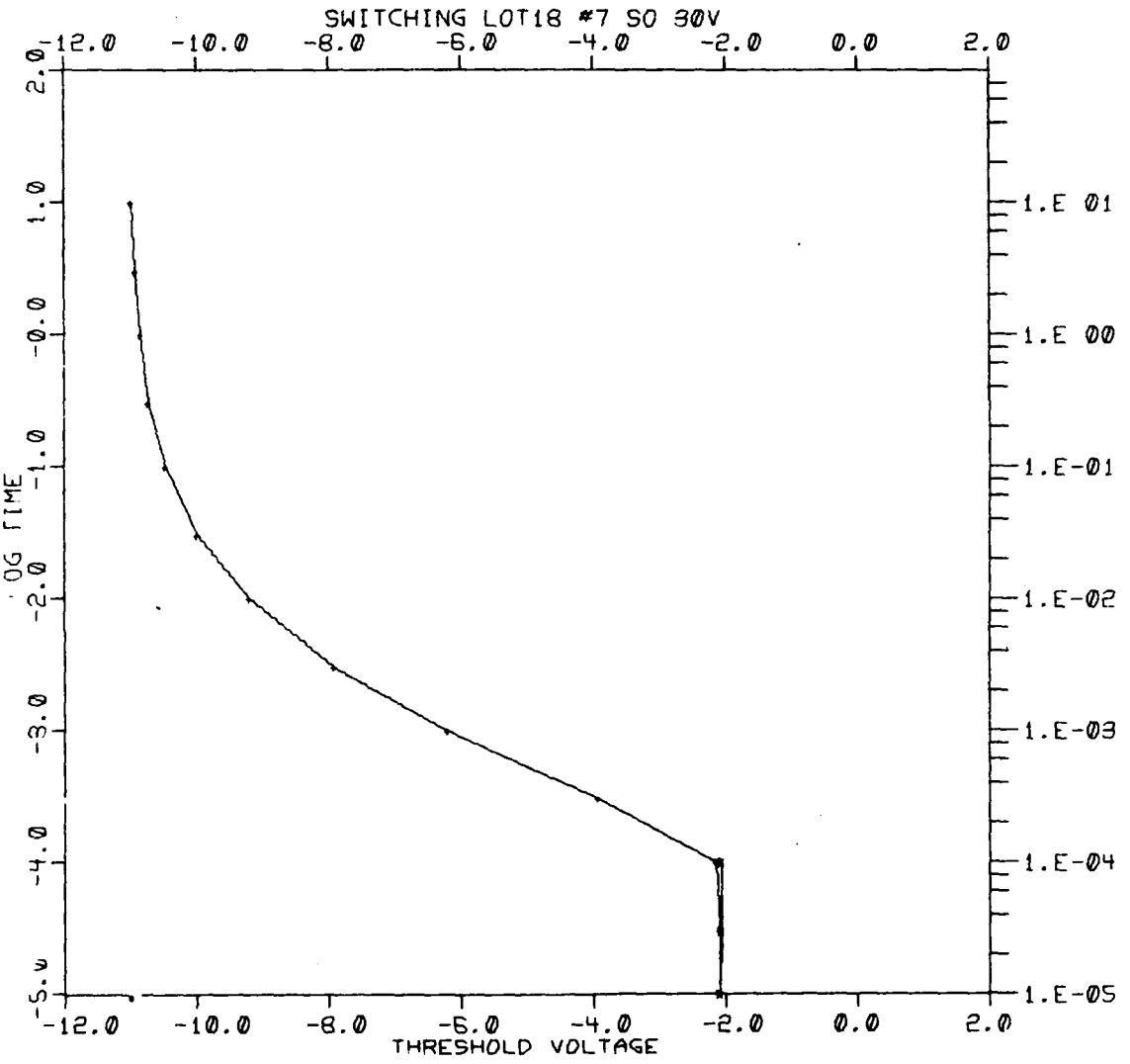

SWITCHING LOT18 #7 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-122

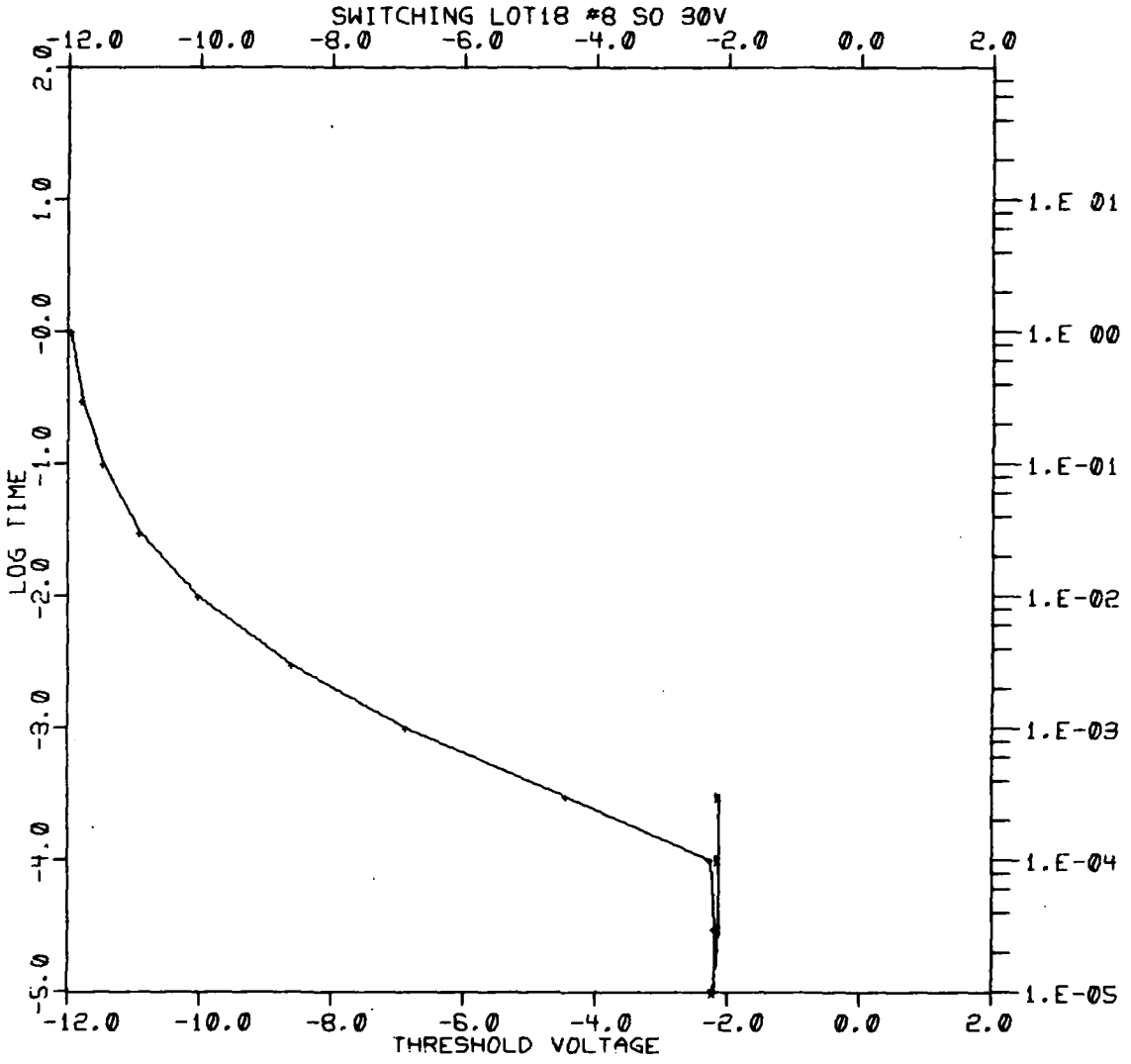

SWITCHING LOT18 #8 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-123

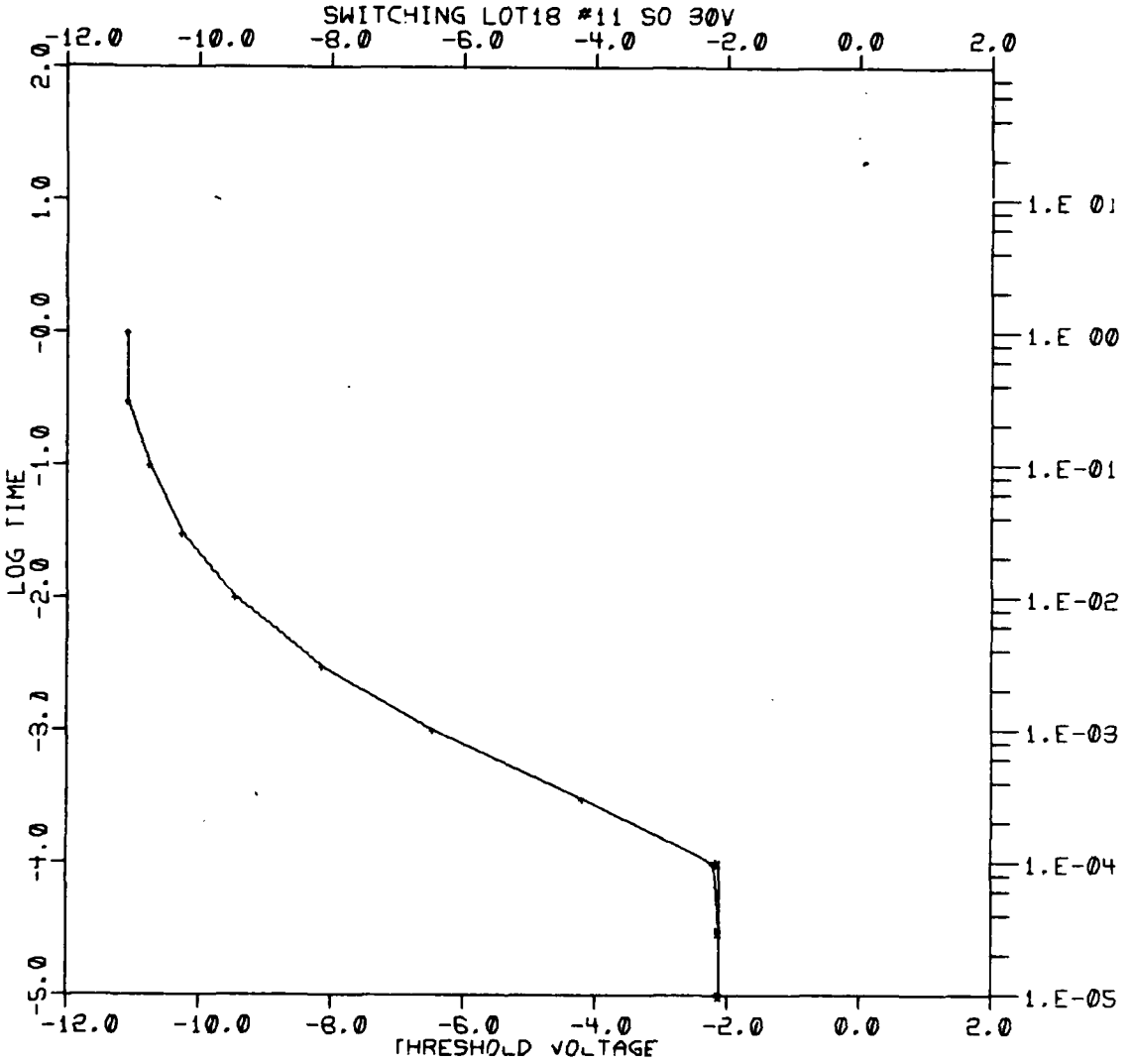

SWITCHING LOT18 #11 SO 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-124

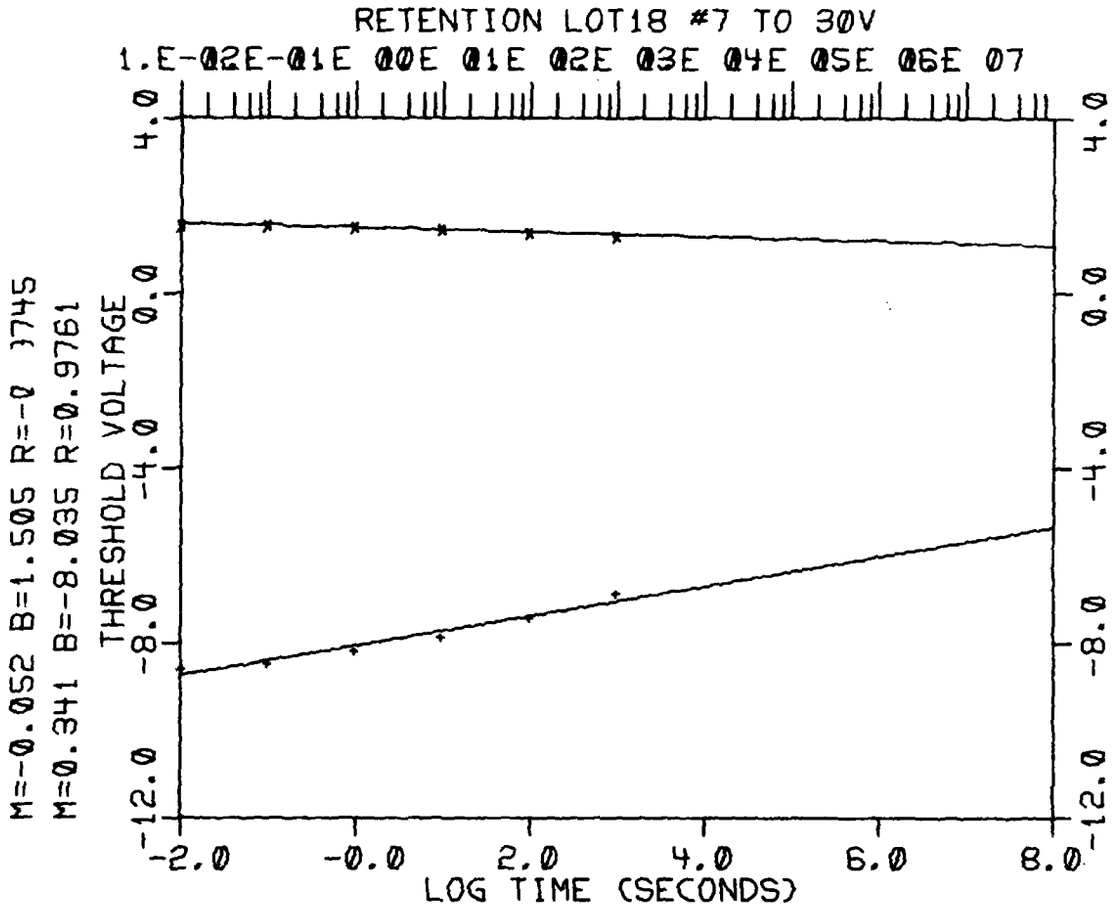

RETENTION LOT18 #7 TO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.052 B=1.505 R=-0 1745
M=0.341 B=-8.035 R=0.9761
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-125

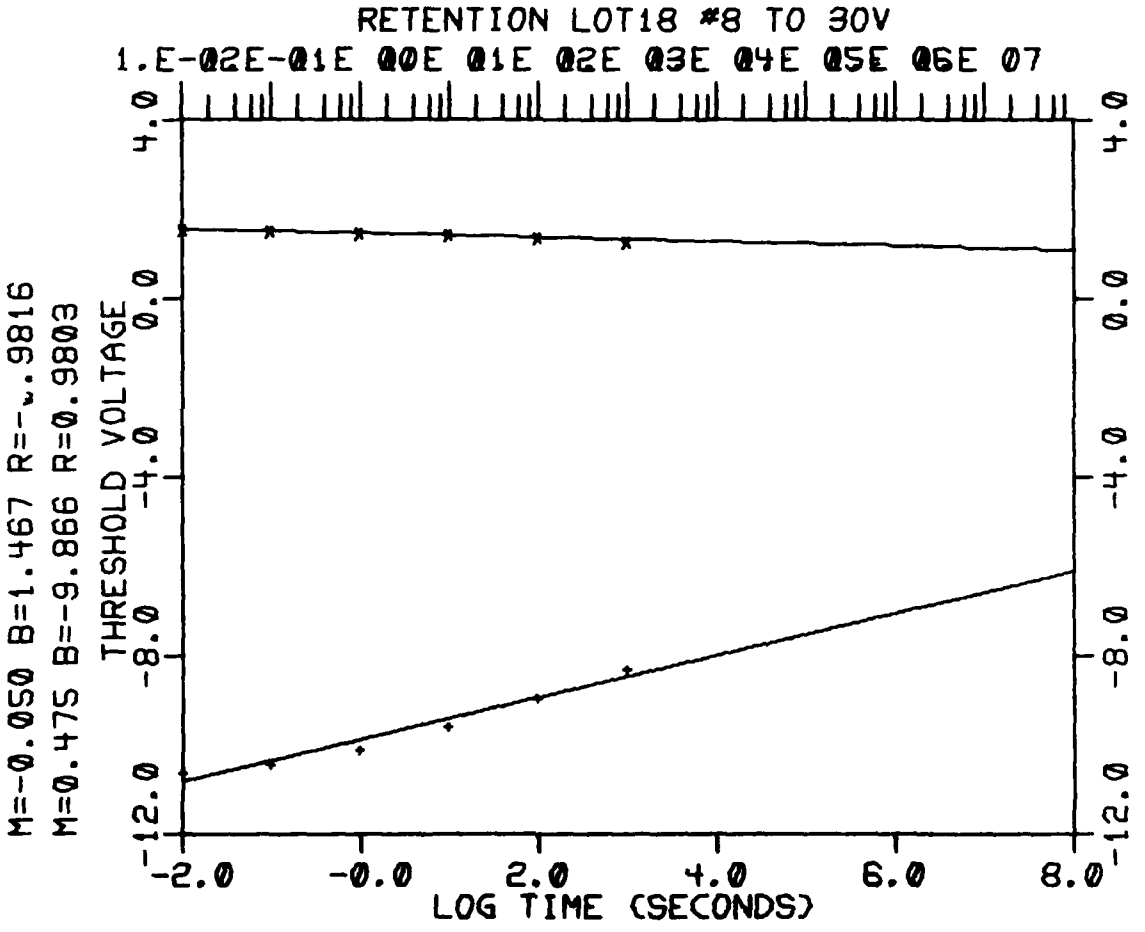

RETENTION LOT18 #8 TO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.050 B=1.467 R=-..9816
M=0.475 B=-9.866 R=0.9803
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-126

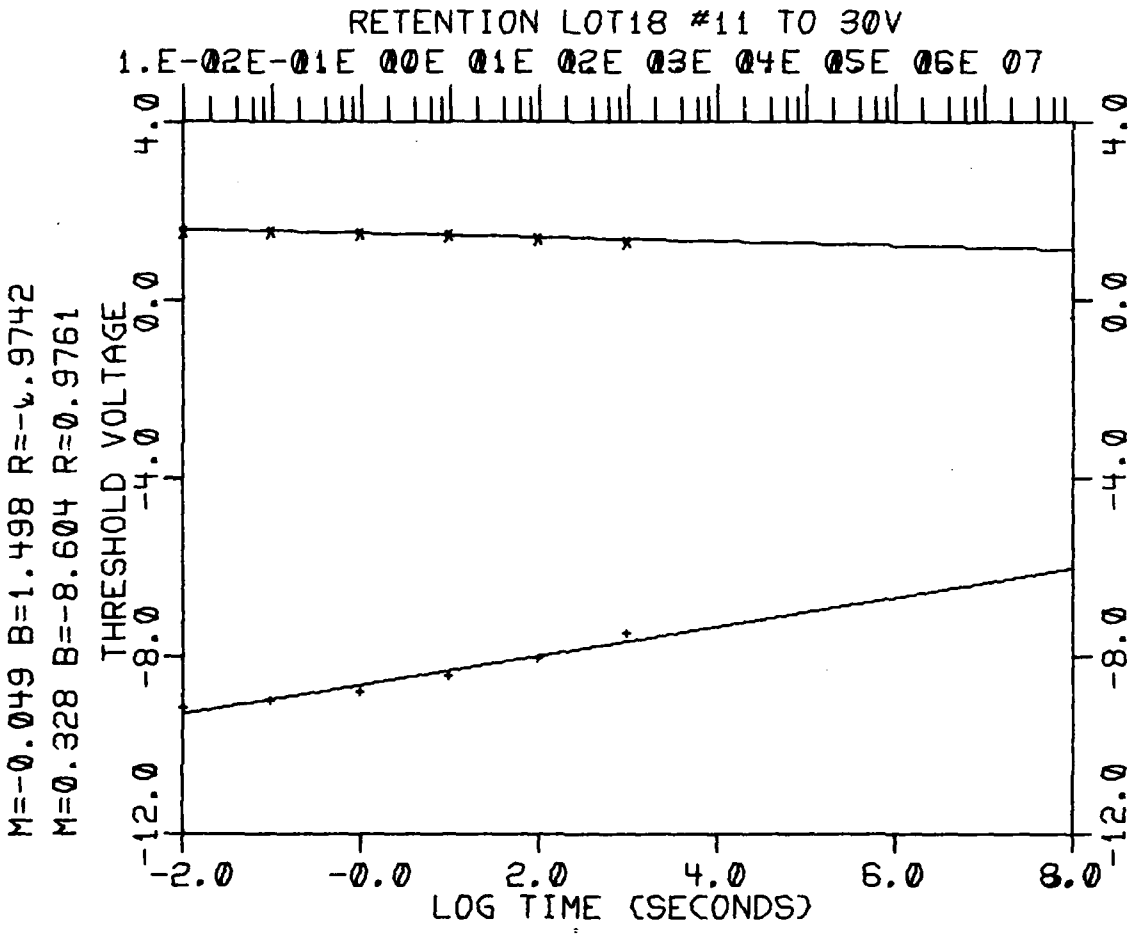

RETENTION LOT18 #11 TO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.049 B=1.498 R=-0.9742
M=0.328 B=-8.604 R=0.9761
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-127

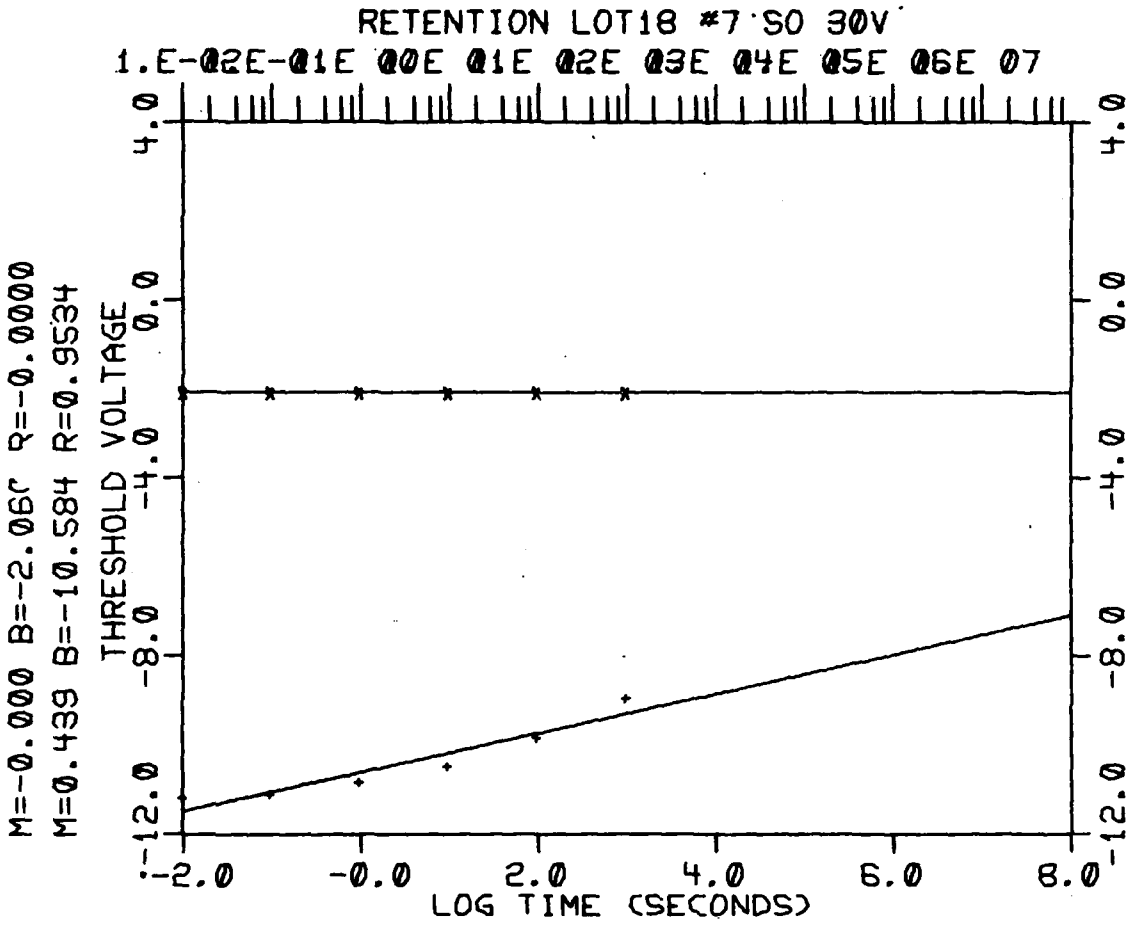

RETENTION LOT18 #7 SO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.067 R=-0.0000
M=0.439 B=-10.584 R=0.9534
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-128

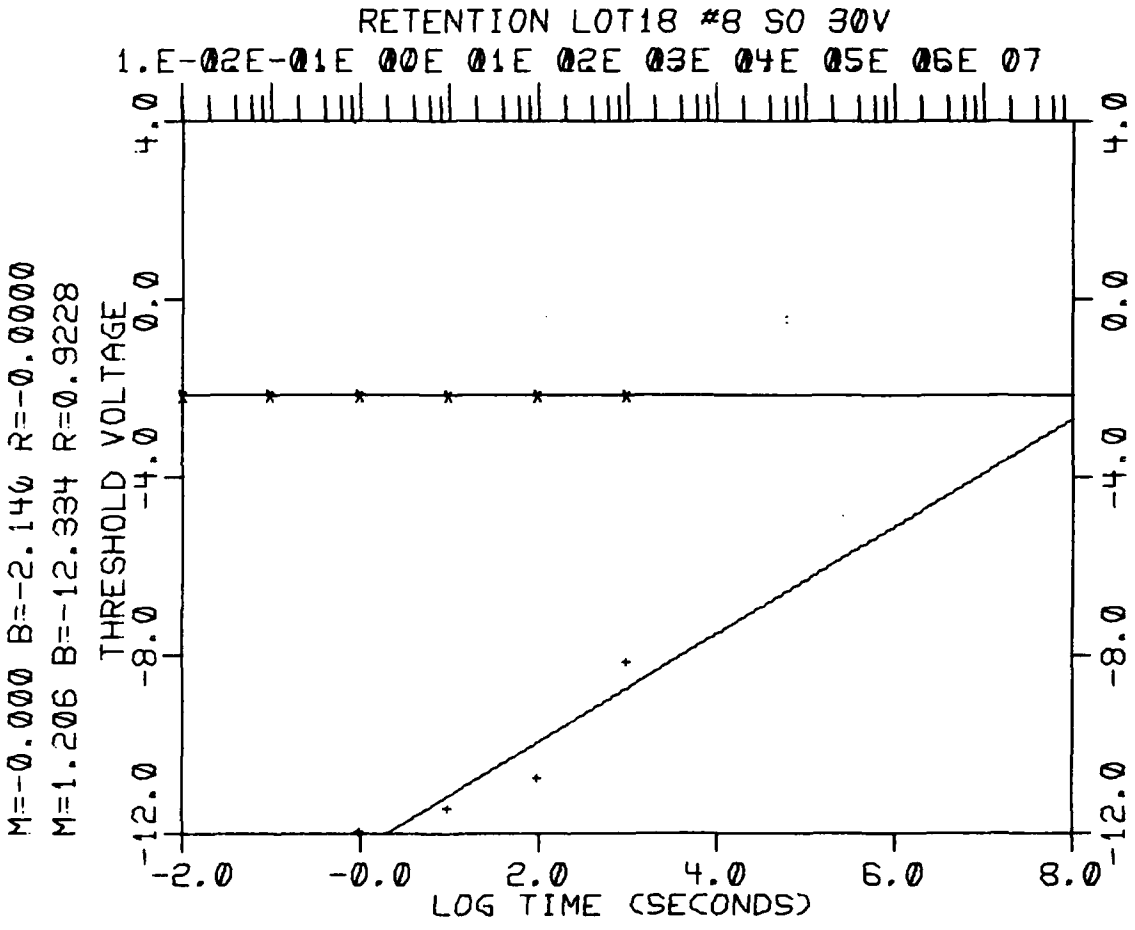

RETENTION LOT18 #8 SO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.146 R=-0.0000
M=1.206 B=-12.334 R=0.9228
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV- 129

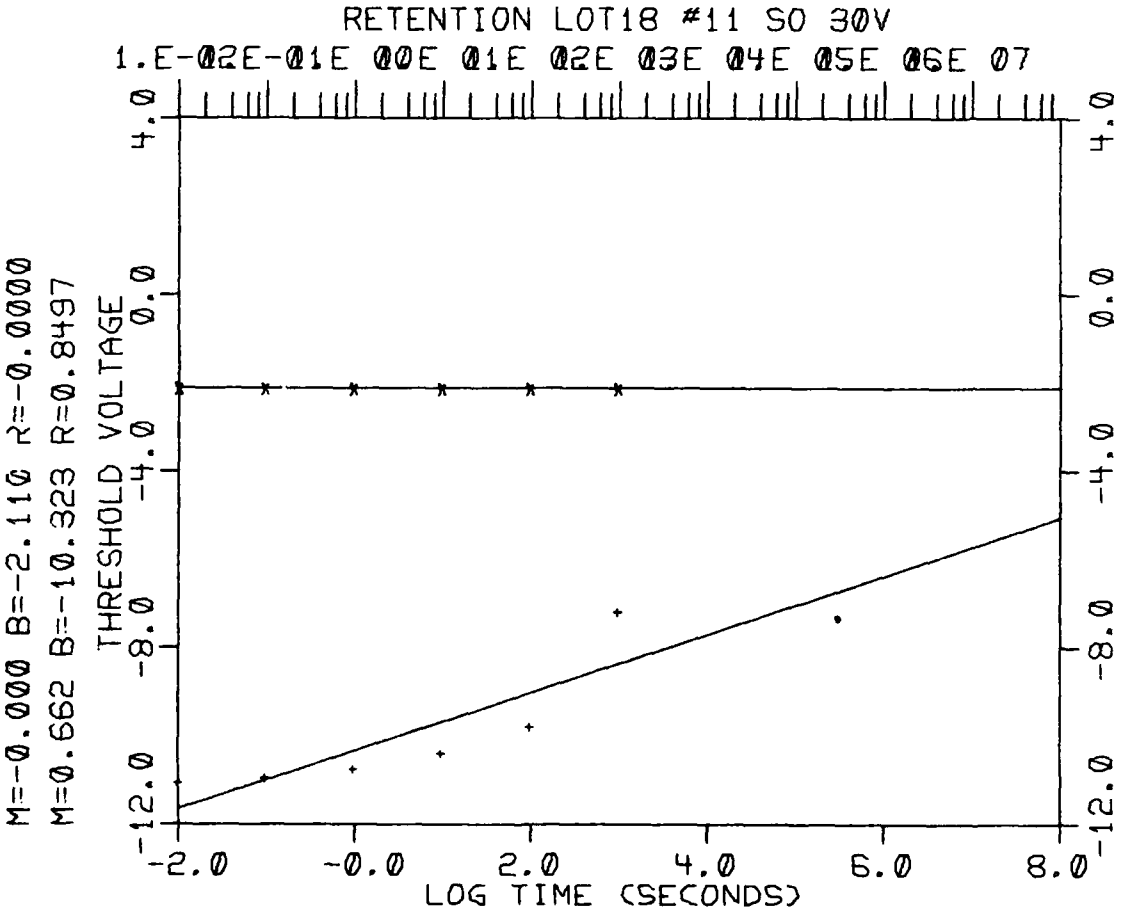

RETENTION LOT18 #11 SO 30V
1.E-02E-01E 00E 01E 02E 03E 04E 05E 06E 07
M=-0.000 B=-2.116 R=-0.0000
M=0.662 B=-10.323 R=0.8497
THRESHOLD VOLTAGE
4.0
0.0
-4.0
-8.0
-12.0
-2.0
-0.0
2.0
4.0
6.0
8.0
LOG TIME (SECONDS)

Fig. IV-130

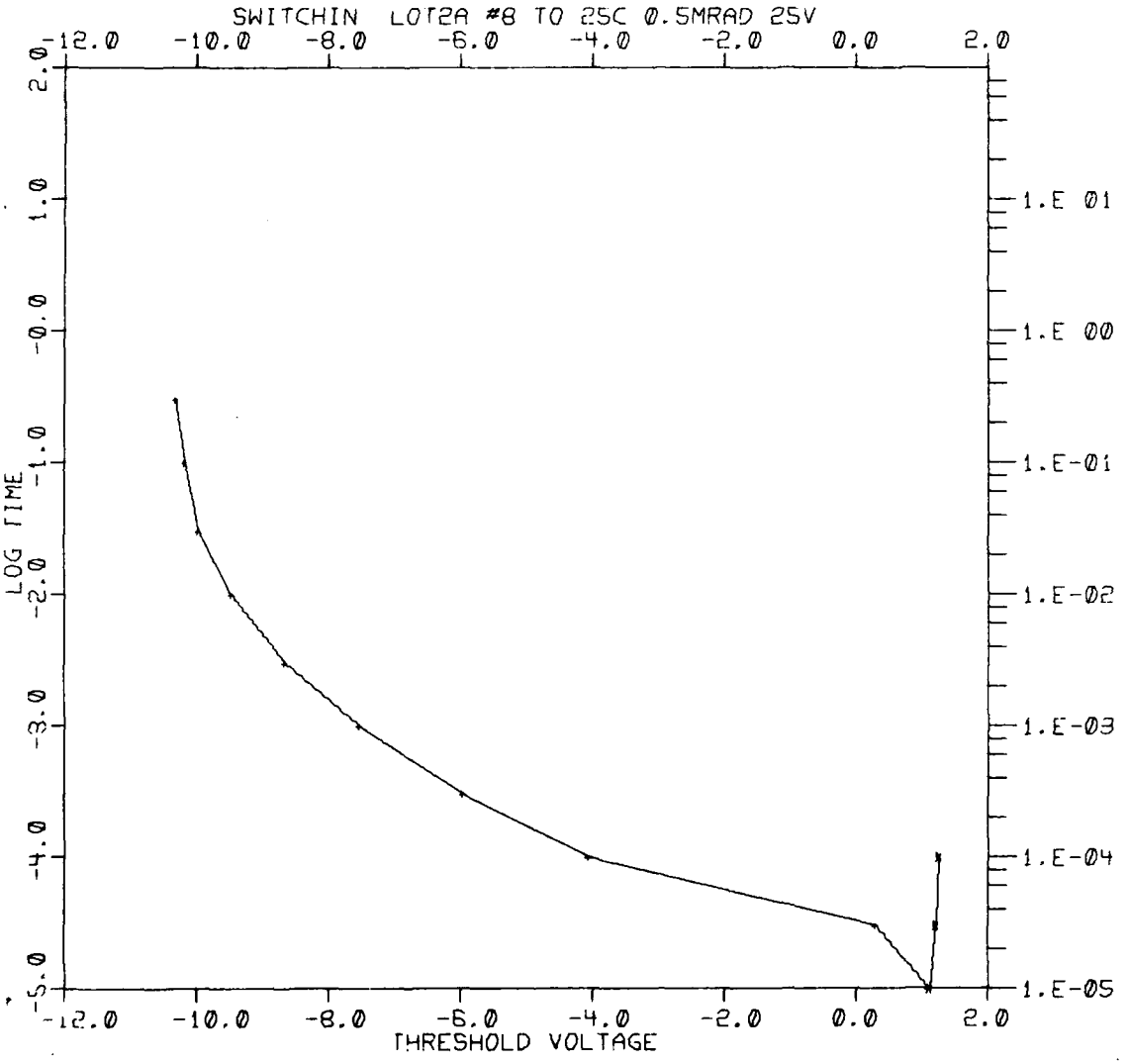

SWITCHIN LOT2A #8 TO 25C 0.5MRAD 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-131

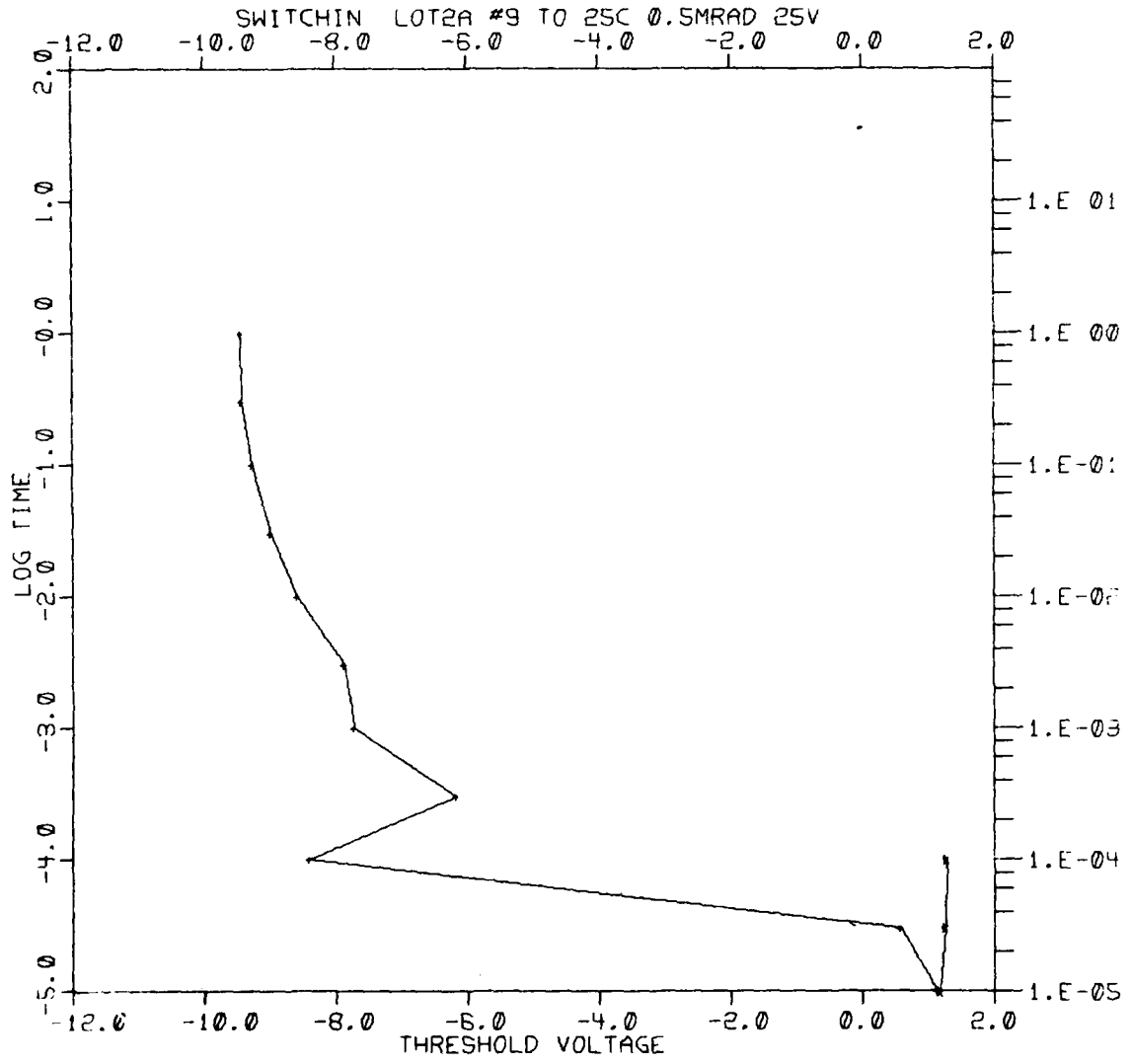

SWITCHIN LOT2A #9 TO 25C 0.5MRAD 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-132

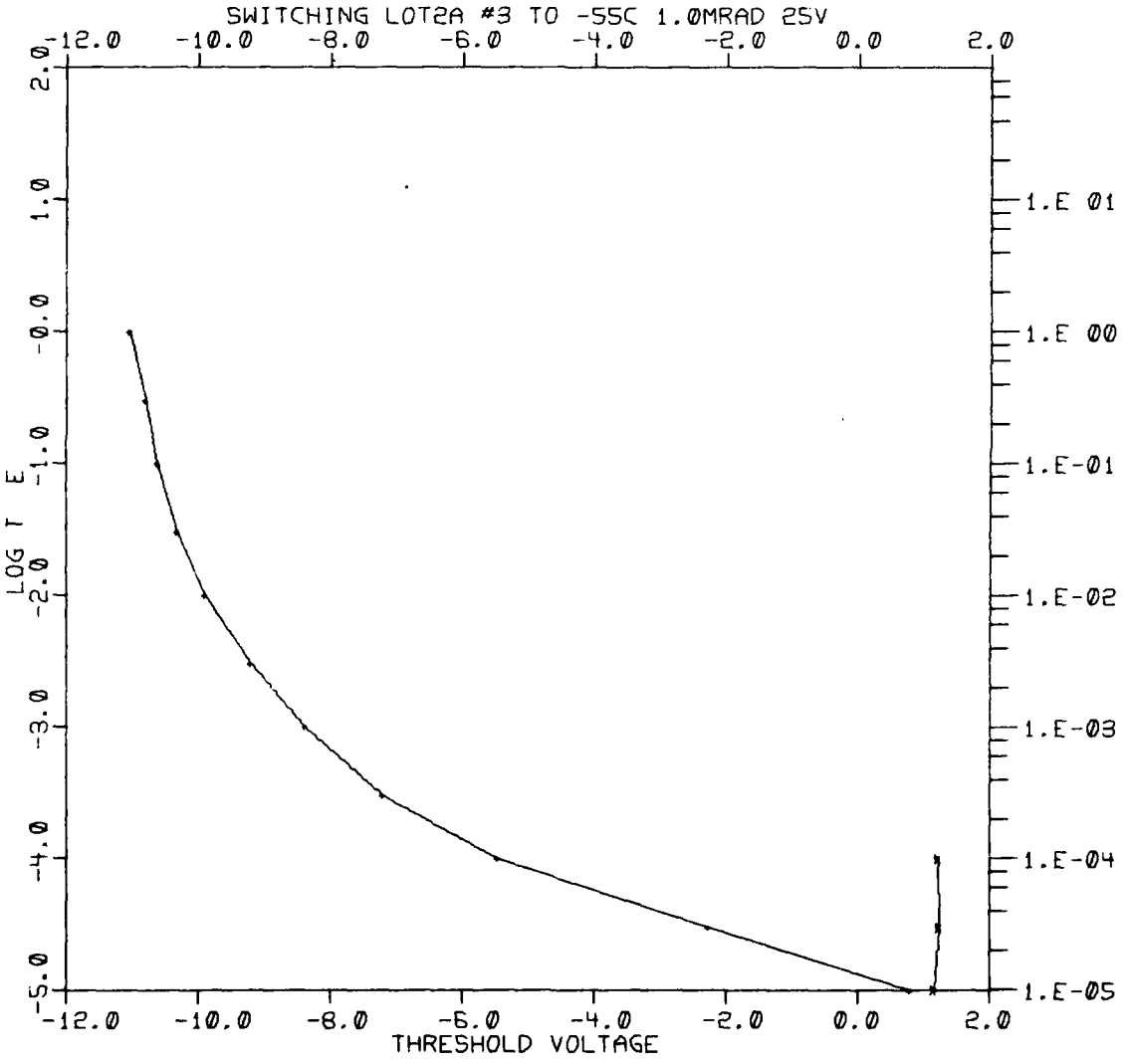

SWITCHING LOT2A #3 TO -55C 1.0MRAD 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG I E
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV- 133

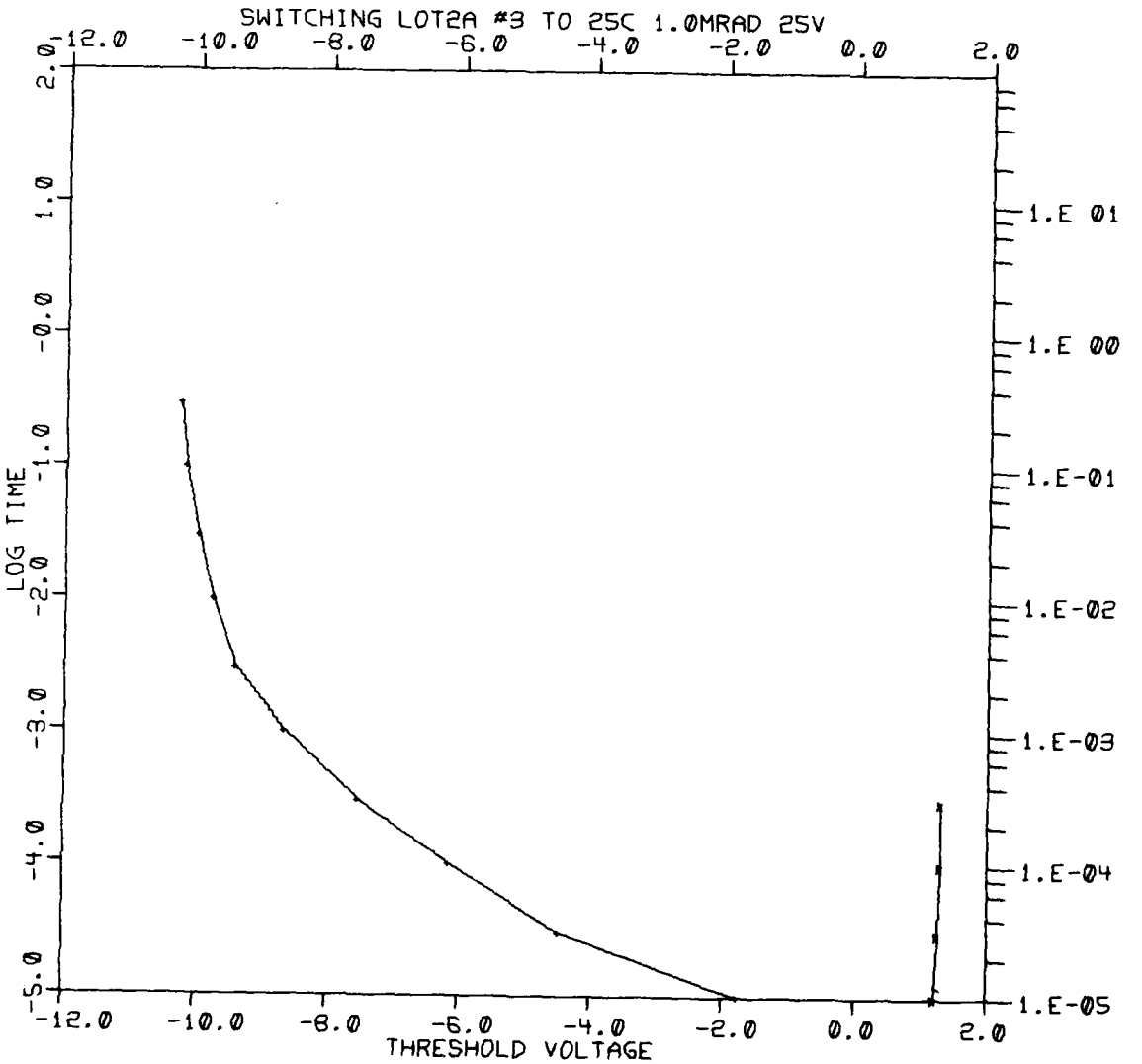

SWITCHING LOT2A #3 TO 25C 1.0MRAD 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-134

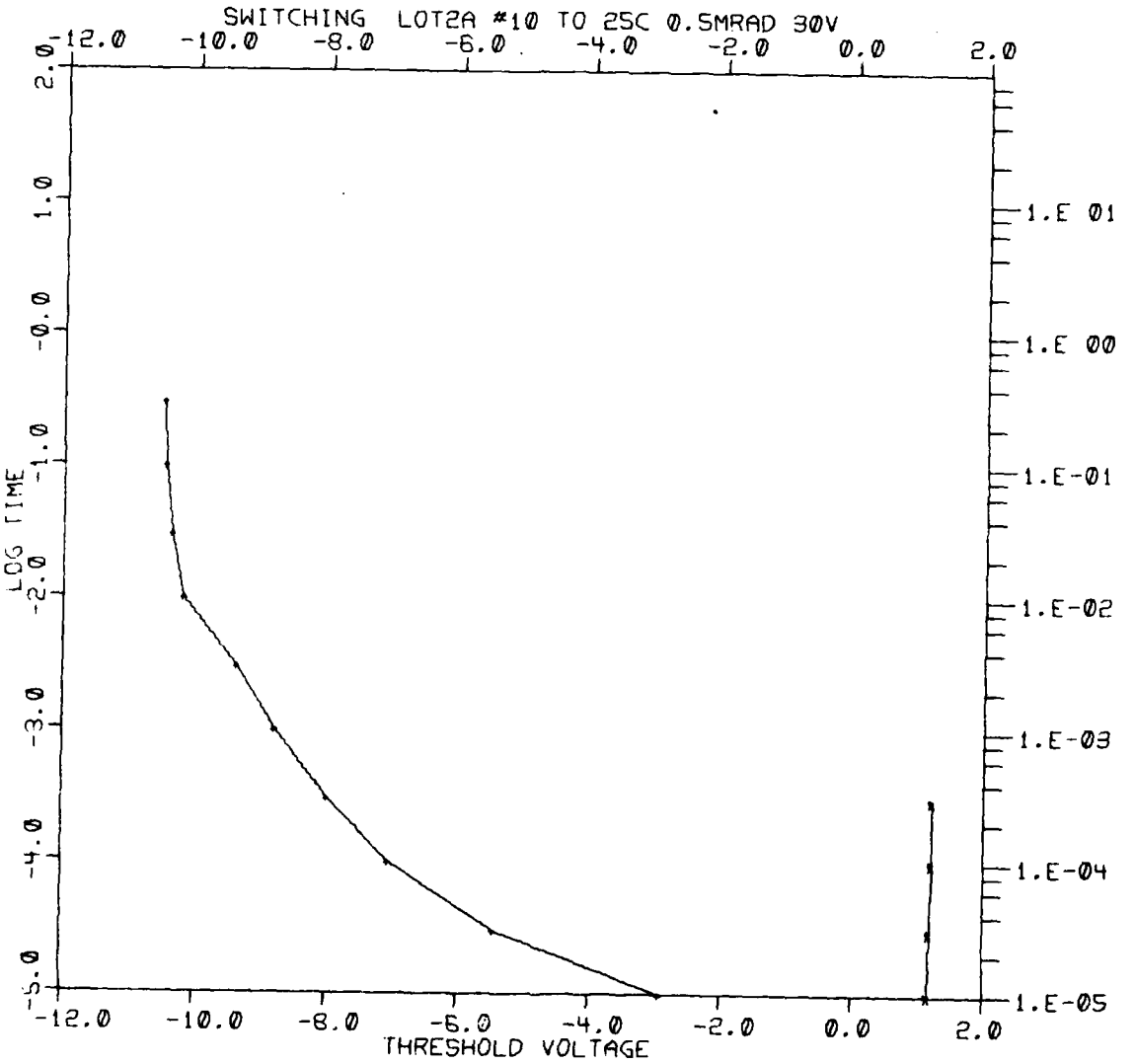

SWITCHING LOT2A #10 TO 25C 0.5MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-135

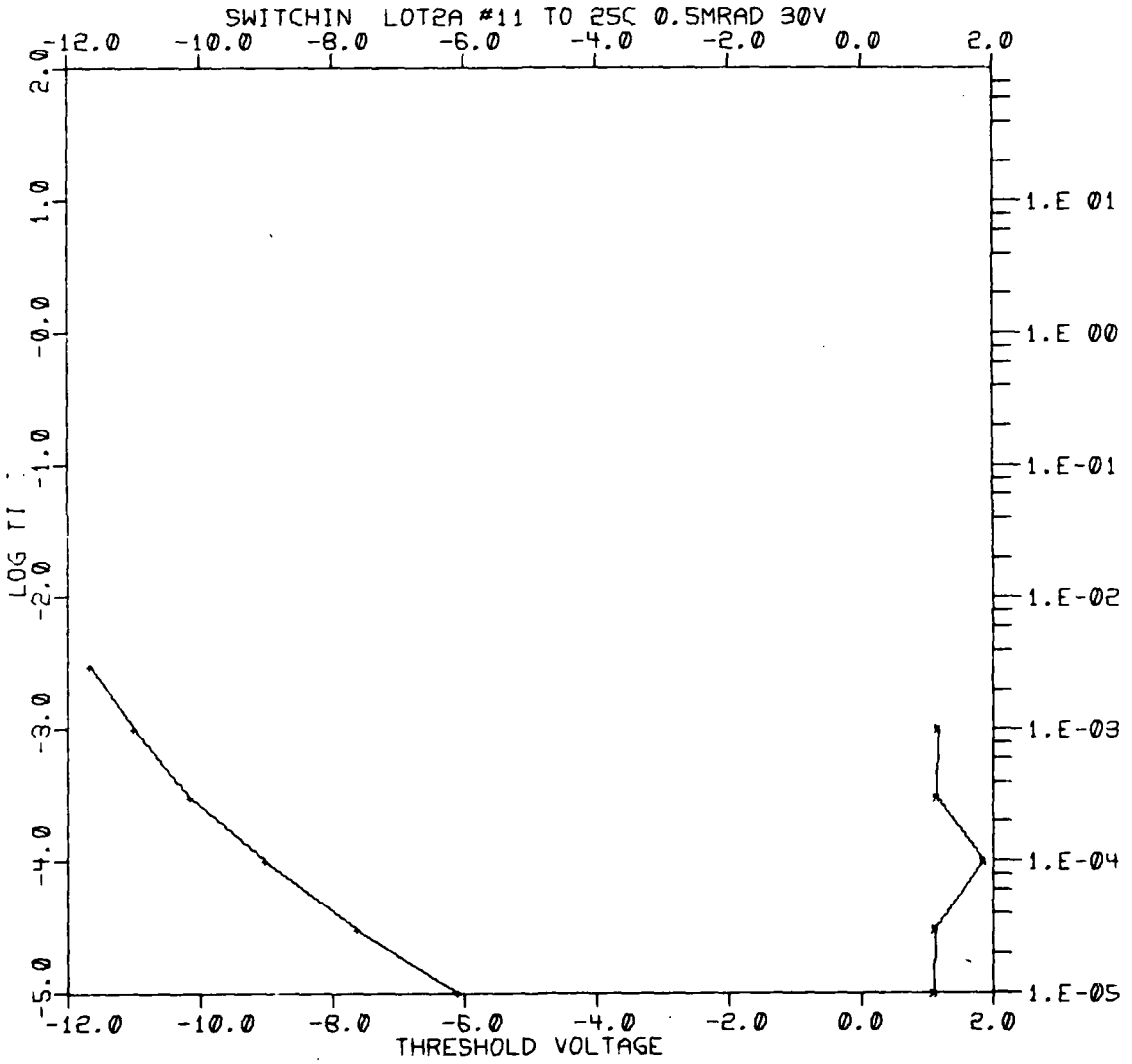

SWITCHIN LOT2A #11 TO 25C 0.5MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG II
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-136

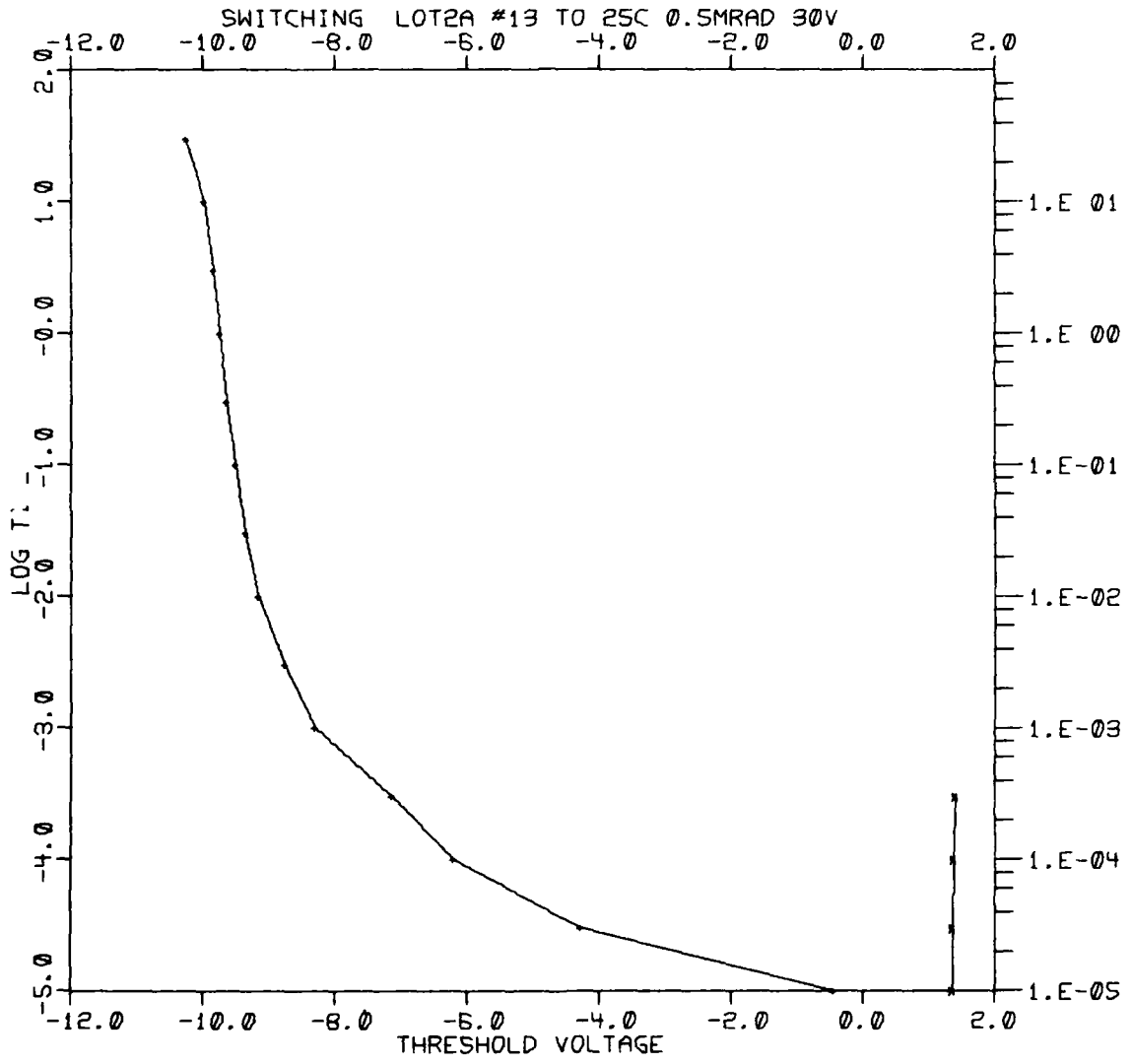

SWITCHING LOT2A #13 TO 25C 0.5MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG T
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-137

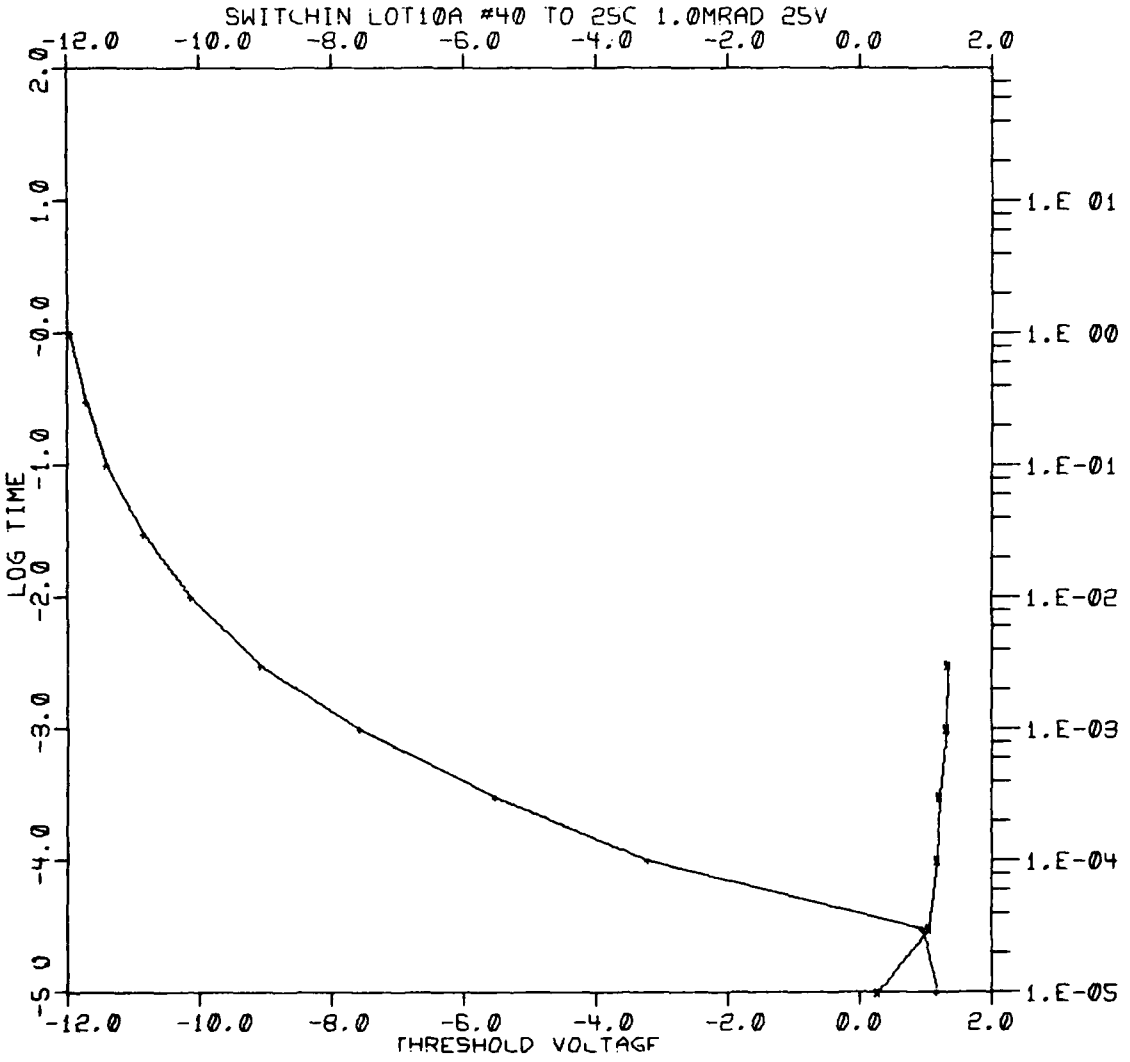

SWITCHIN LOT10A #40 TO 25C 1.0MRAD 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-138

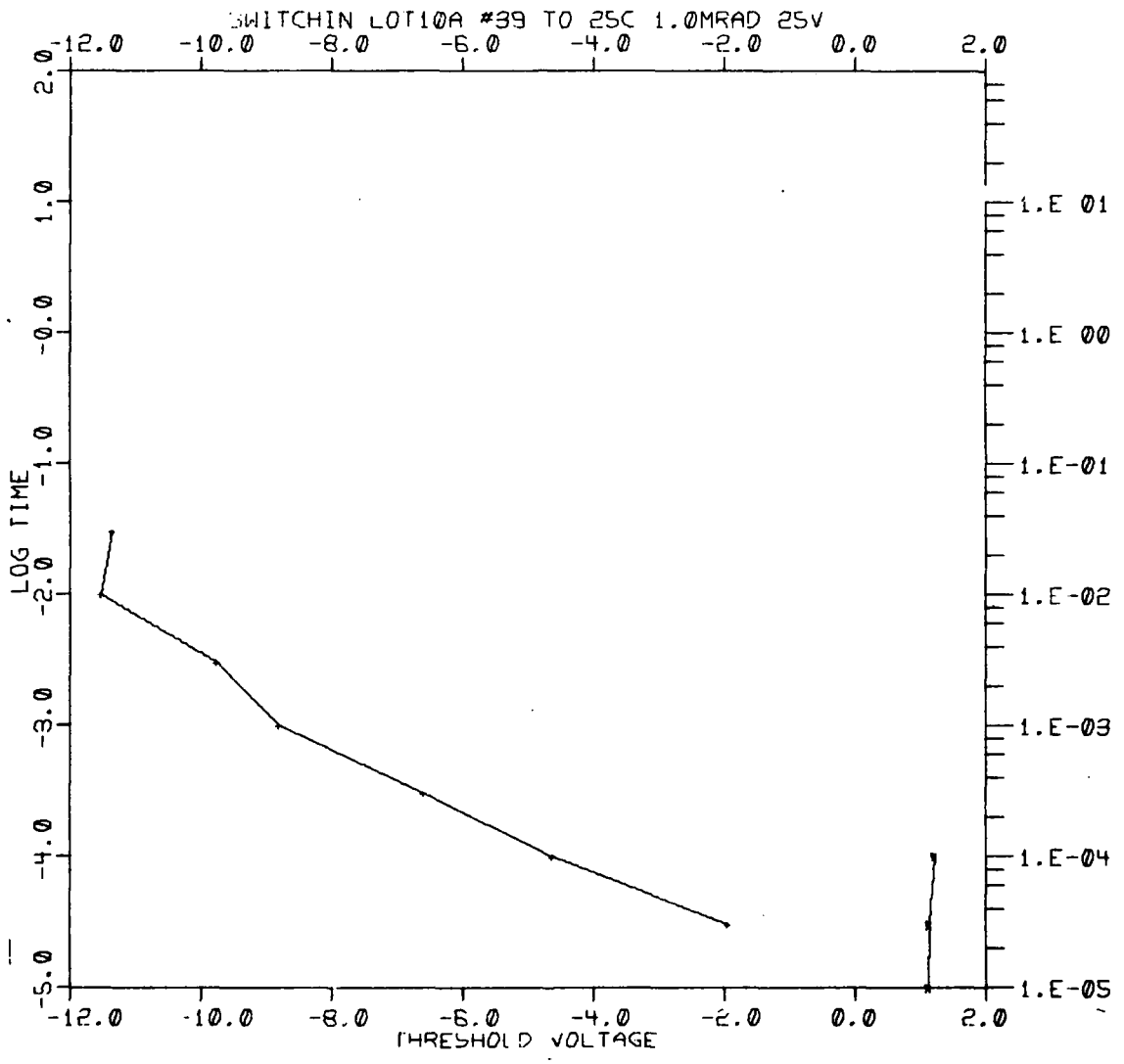

SWITCHIN LOT10A #39 TO 25C 1.0MRAD 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-139

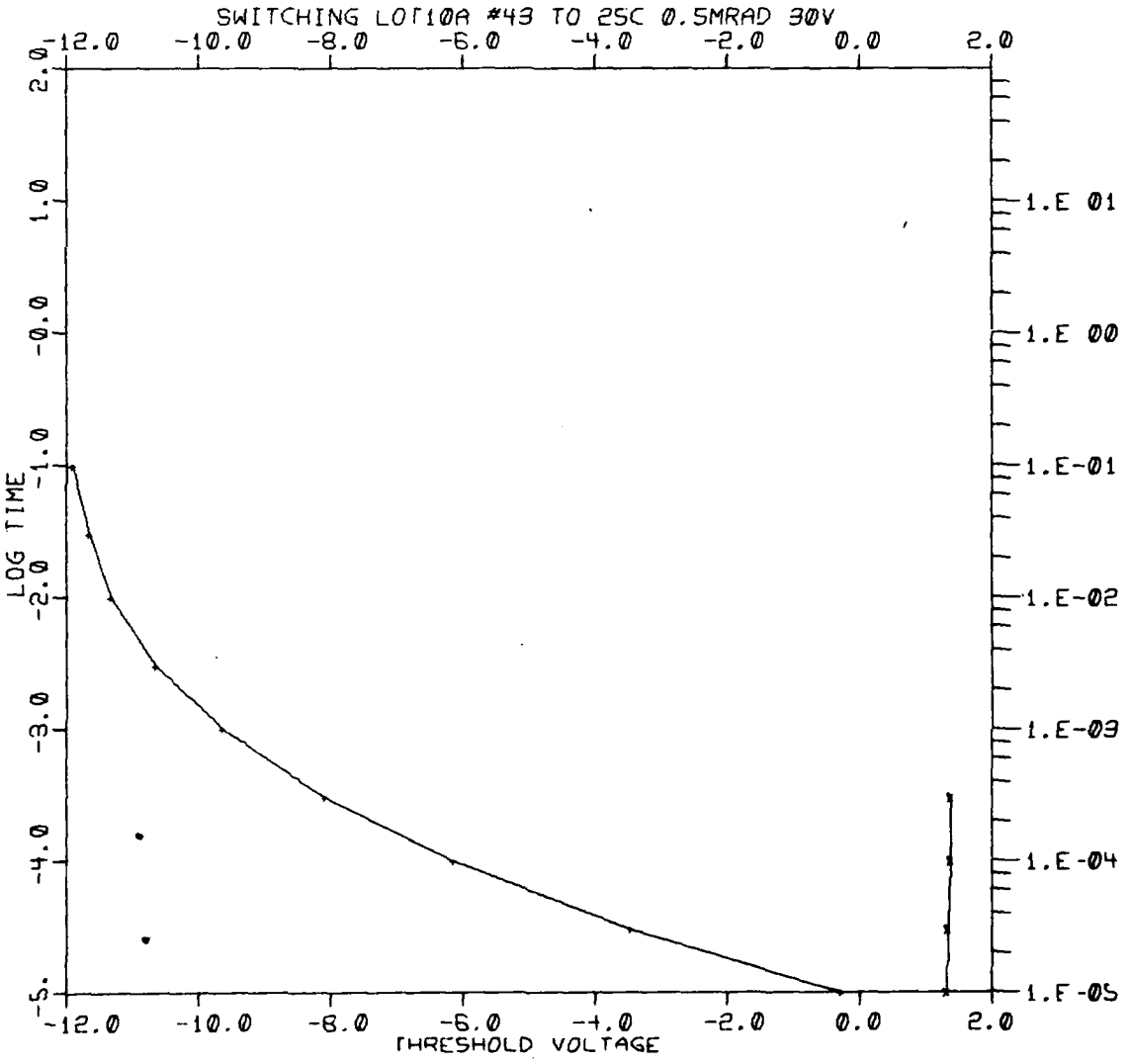

SWITCHING LOT10A #43 TO 25C 0.5MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-140

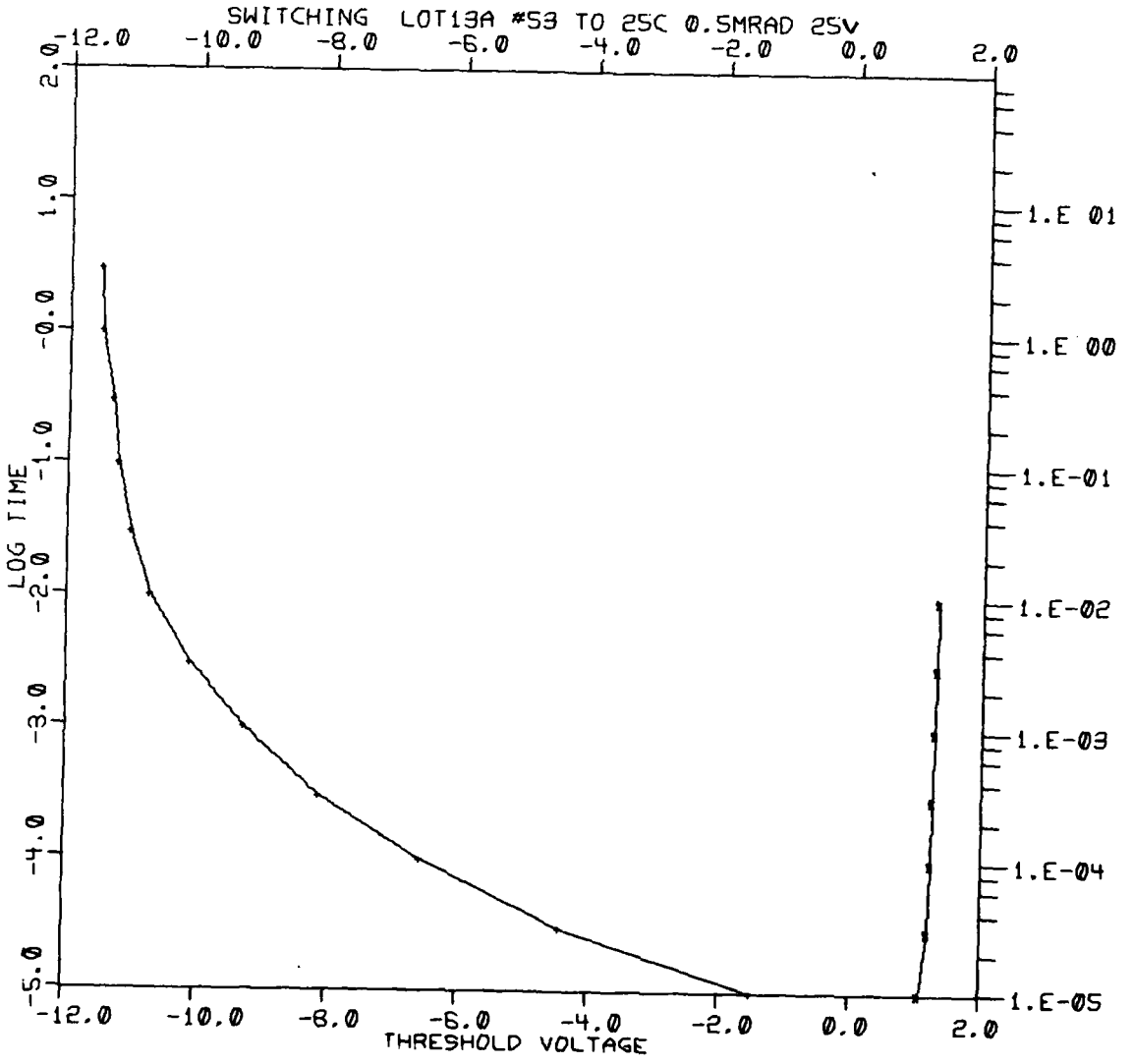

SWITCHING LOT13A #53 TO 25C 0.5MRAD 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV- 141

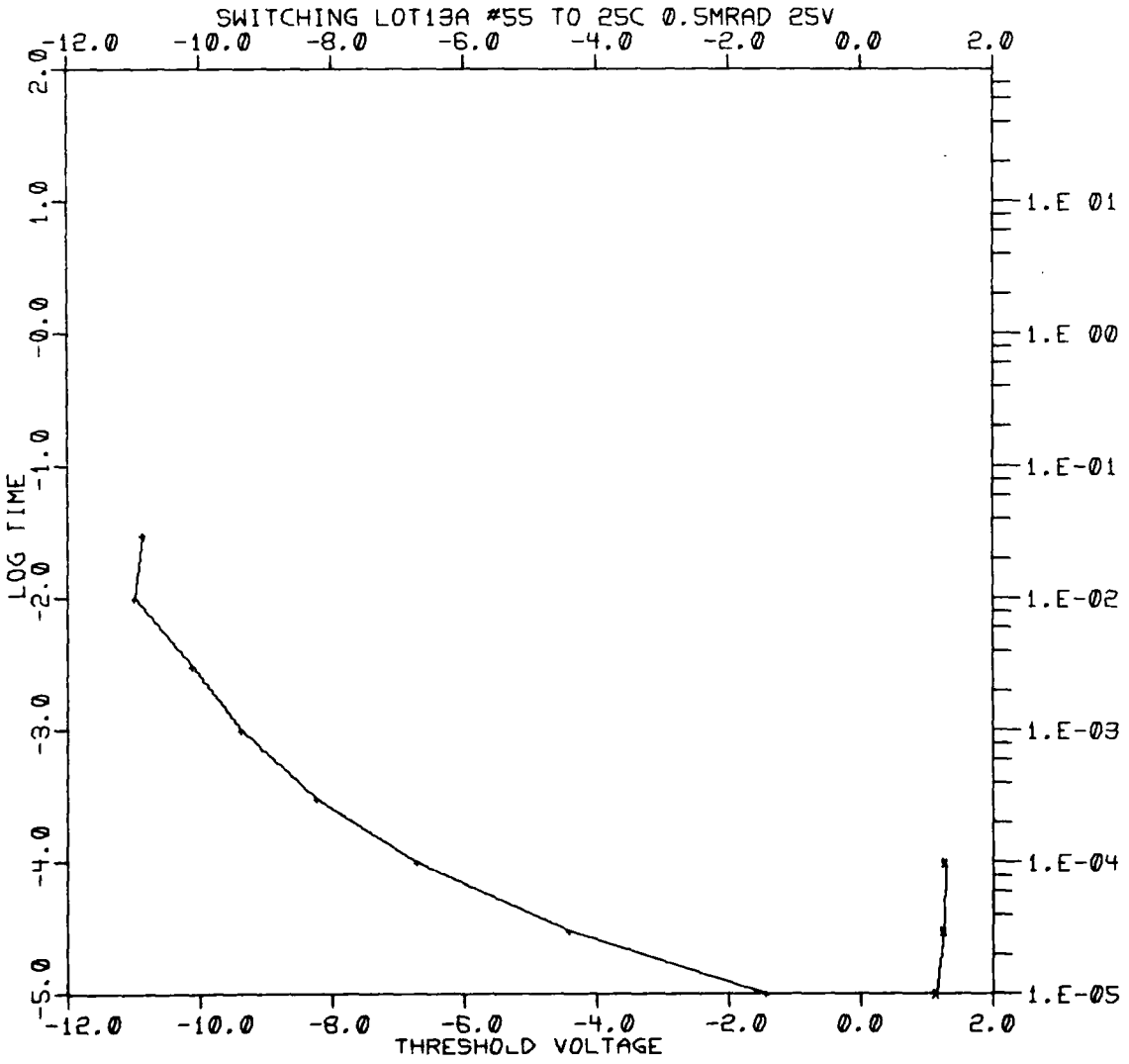

SWITCHING LOT13A #55 TO 25C 0.5MRAD 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-142

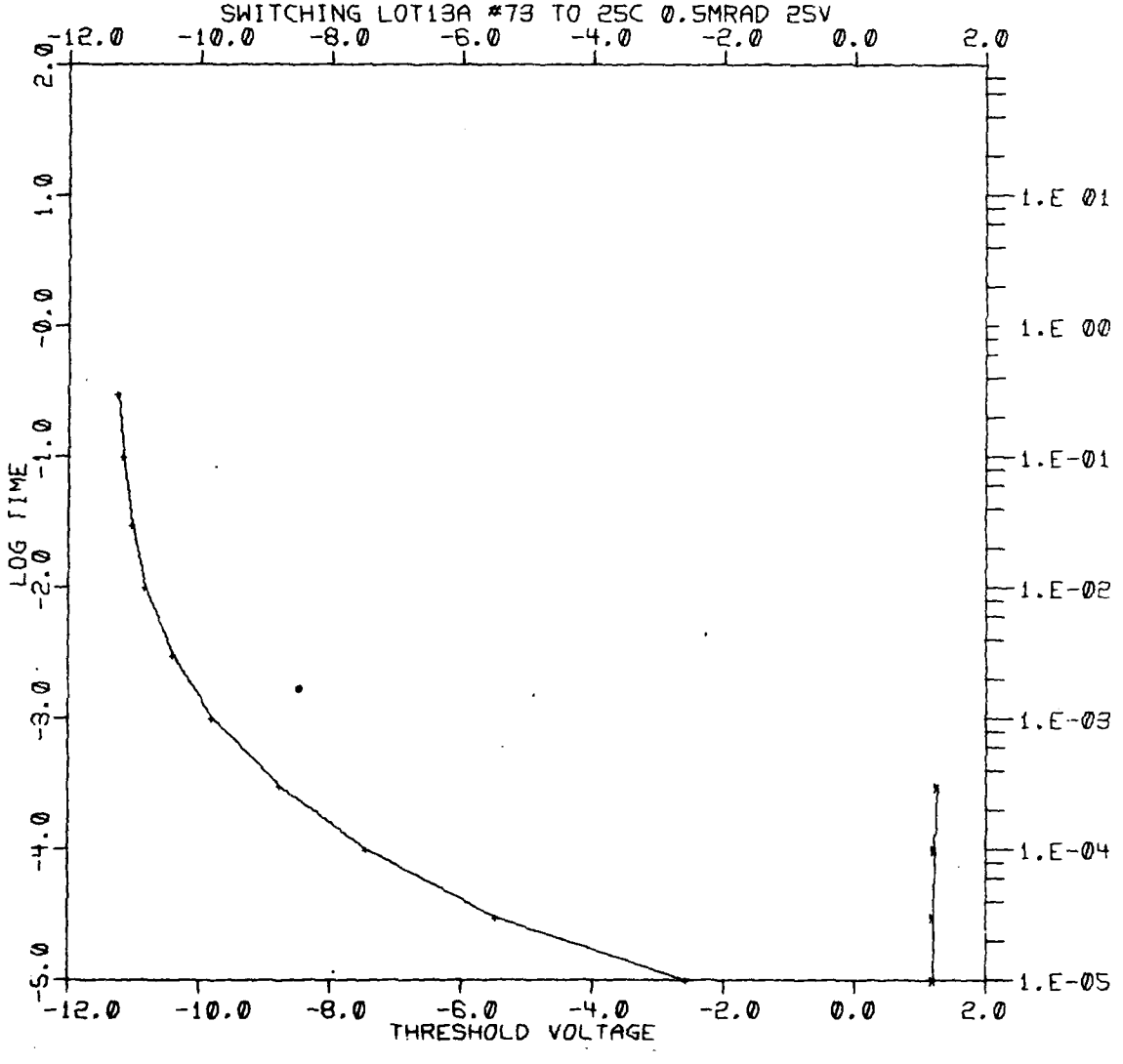

SWITCHING LOT13A #73 TO 25C 0.5MRAD 2SV
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-143

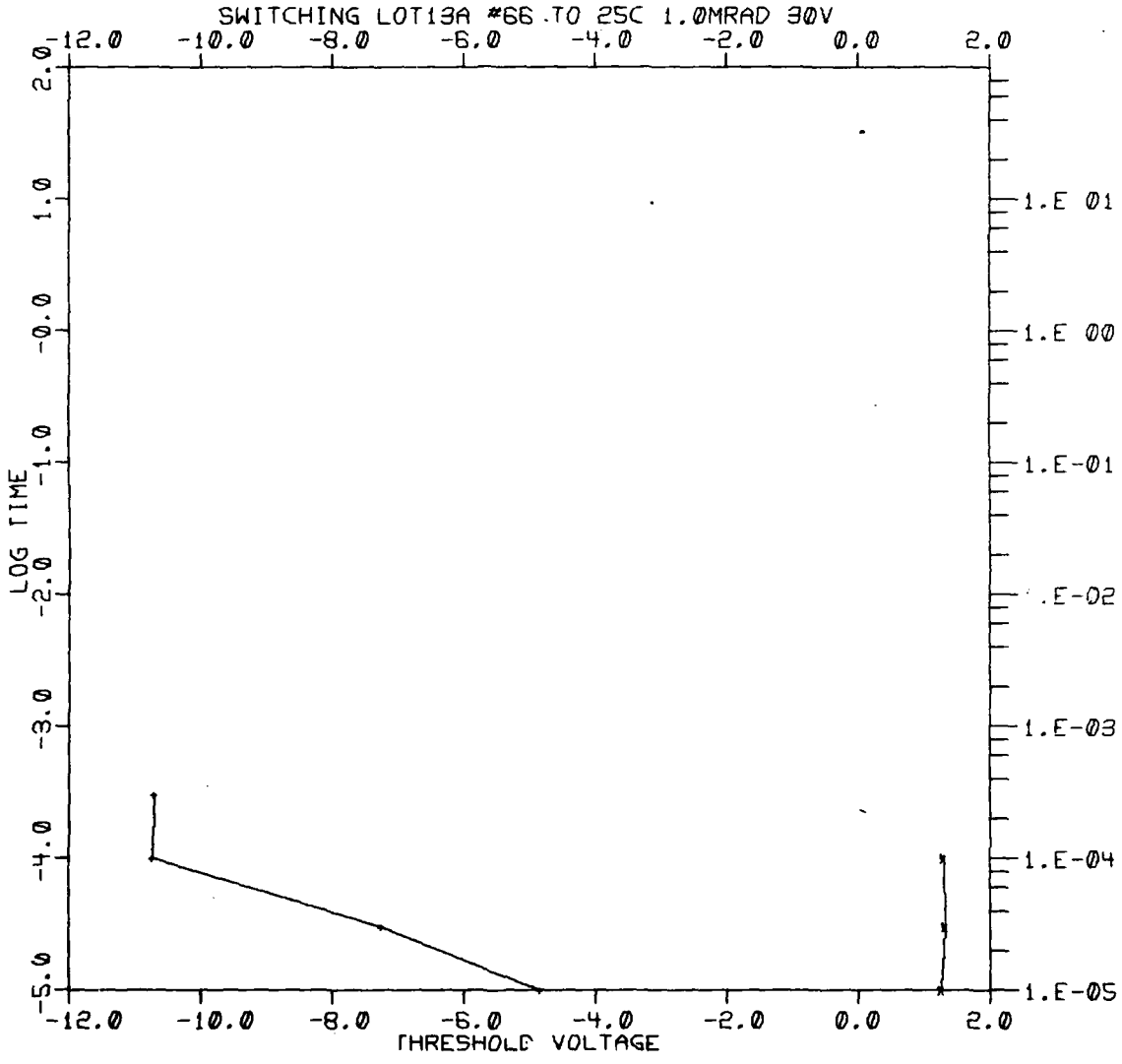

SWITCHING LOT13A #66 TO 25C 1.0MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-144

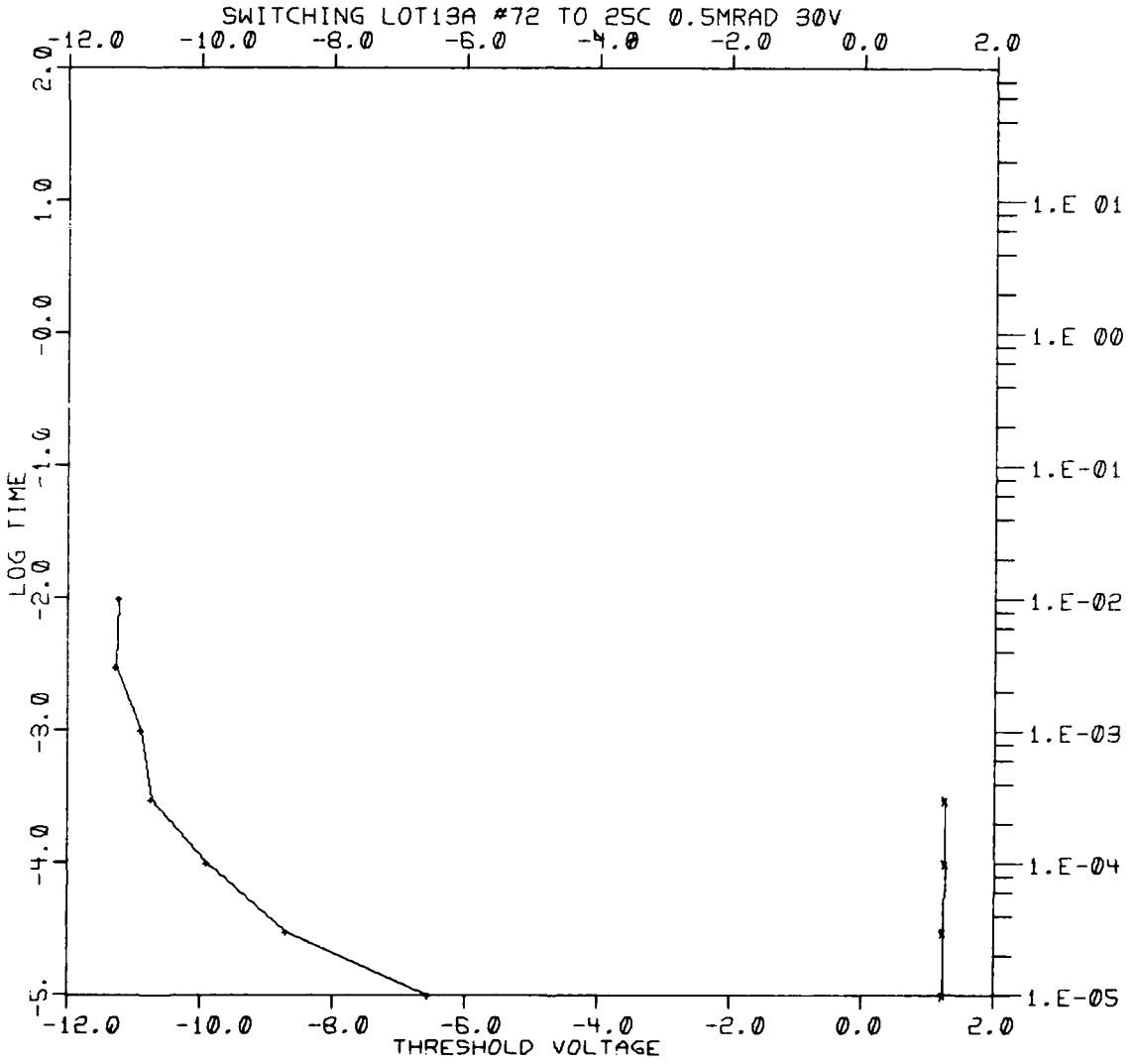

SWITCHING LOT13A #72 TO 25C 0.5MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-145

AD-A091 952 RCA SOLID STATE DIV SOMERVILLE NJ F/G 9/5
FEASIBILITY STUDY OF THE COMBINATION OF MNOS ELEMENTS AND BIPOL--ETC(U)
AUG 80 K CUNNIFF F19628-78-C-0178
UNCLASSIFIED RADC-TR-80-177 NL

3 of 3
AD A091952

END
DATE FILMED
1-81
DTIC

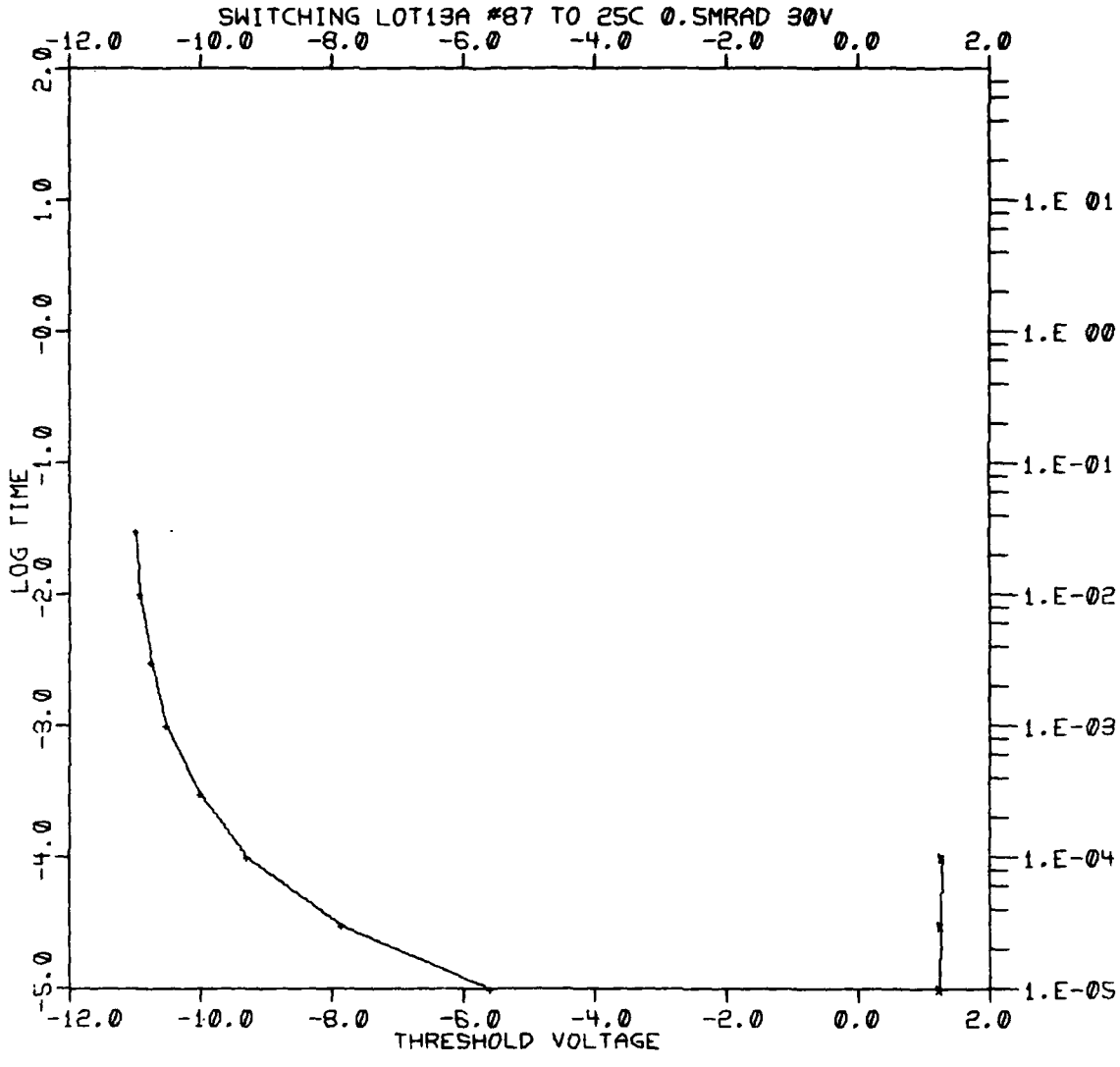

SWITCHING LOT13A #87 TO 25C 0.5MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-146

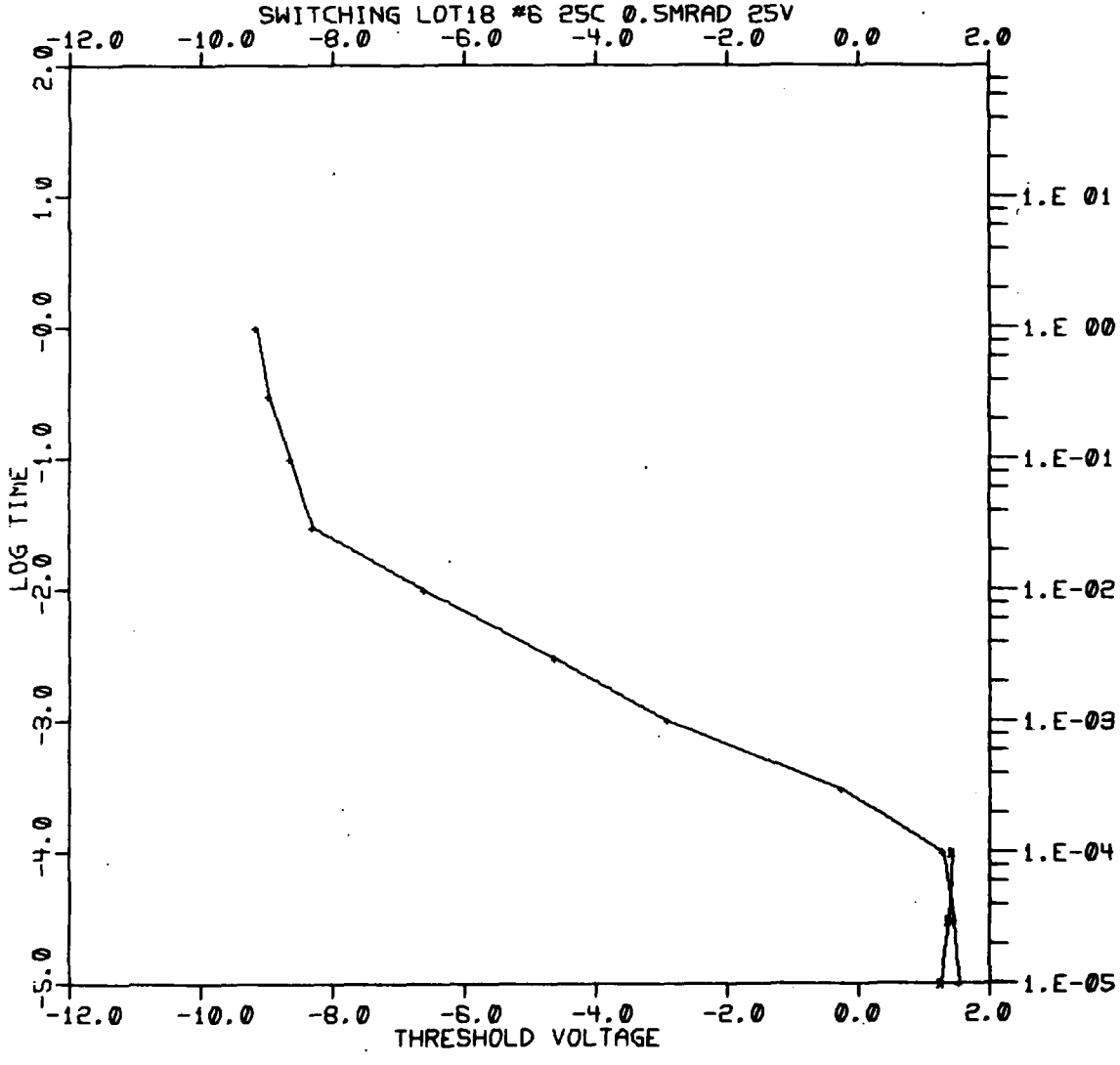

SWITCHING LOT18 #6 25C 0.5MRAD 25V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-147

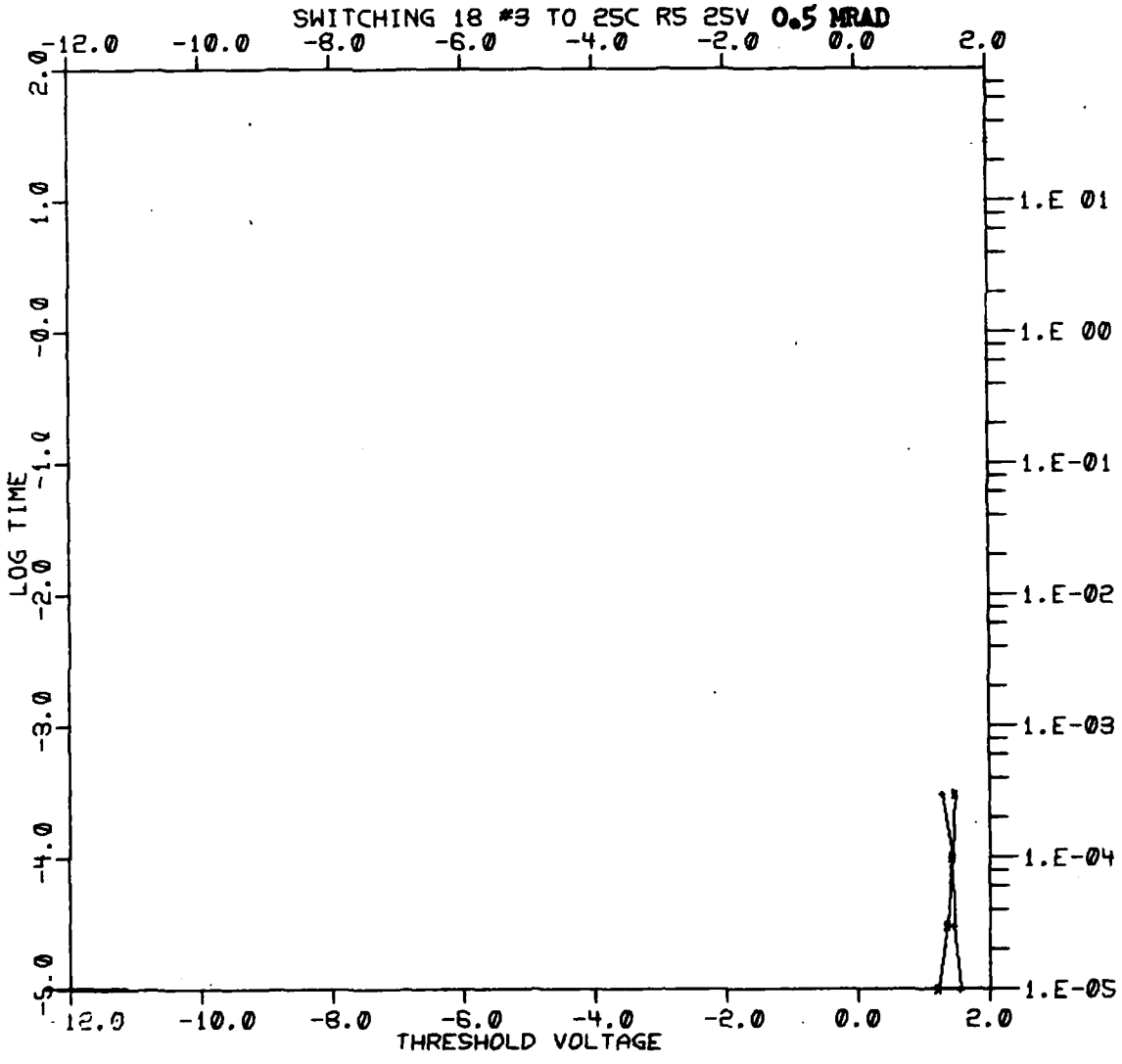

SWITCHING 18 #3 TO 25C R5 25V 0.5 MRAD
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TIME
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-148

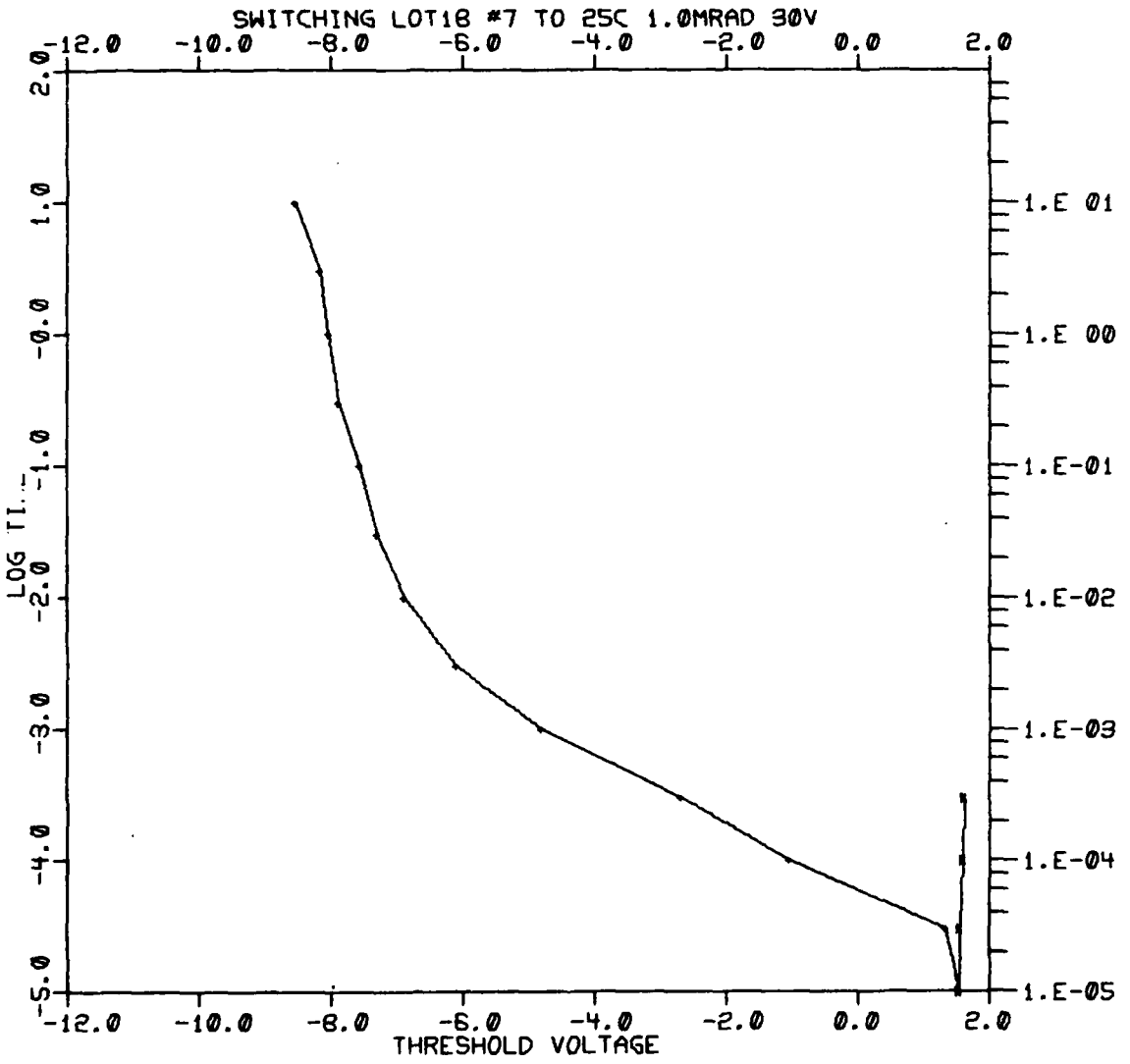

SWITCHING LOT18 #7 TO 25C 1.0MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TI
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-149

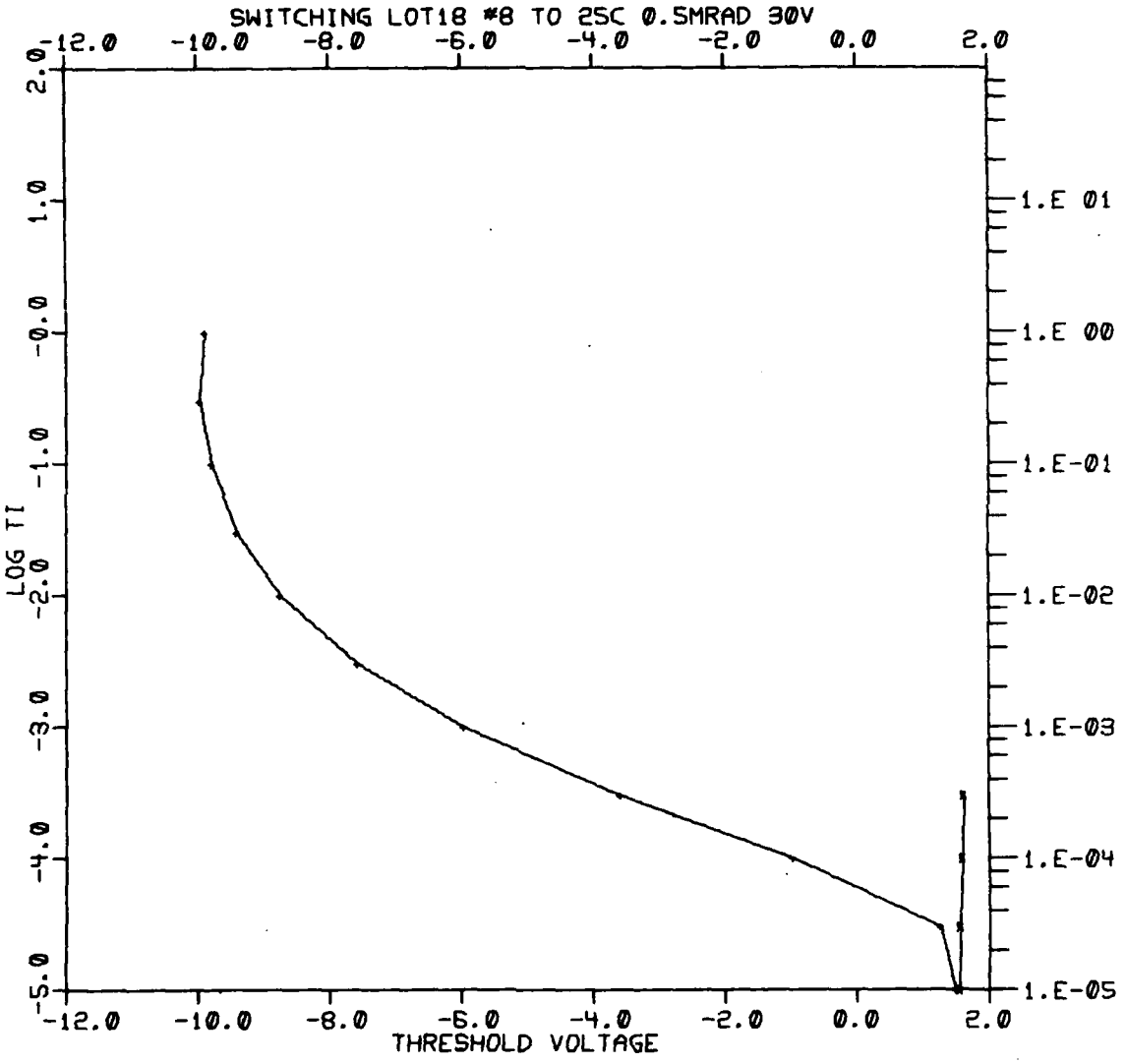

SWITCHING LOT18 #8 TO 25C 0.5MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG TI
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-150

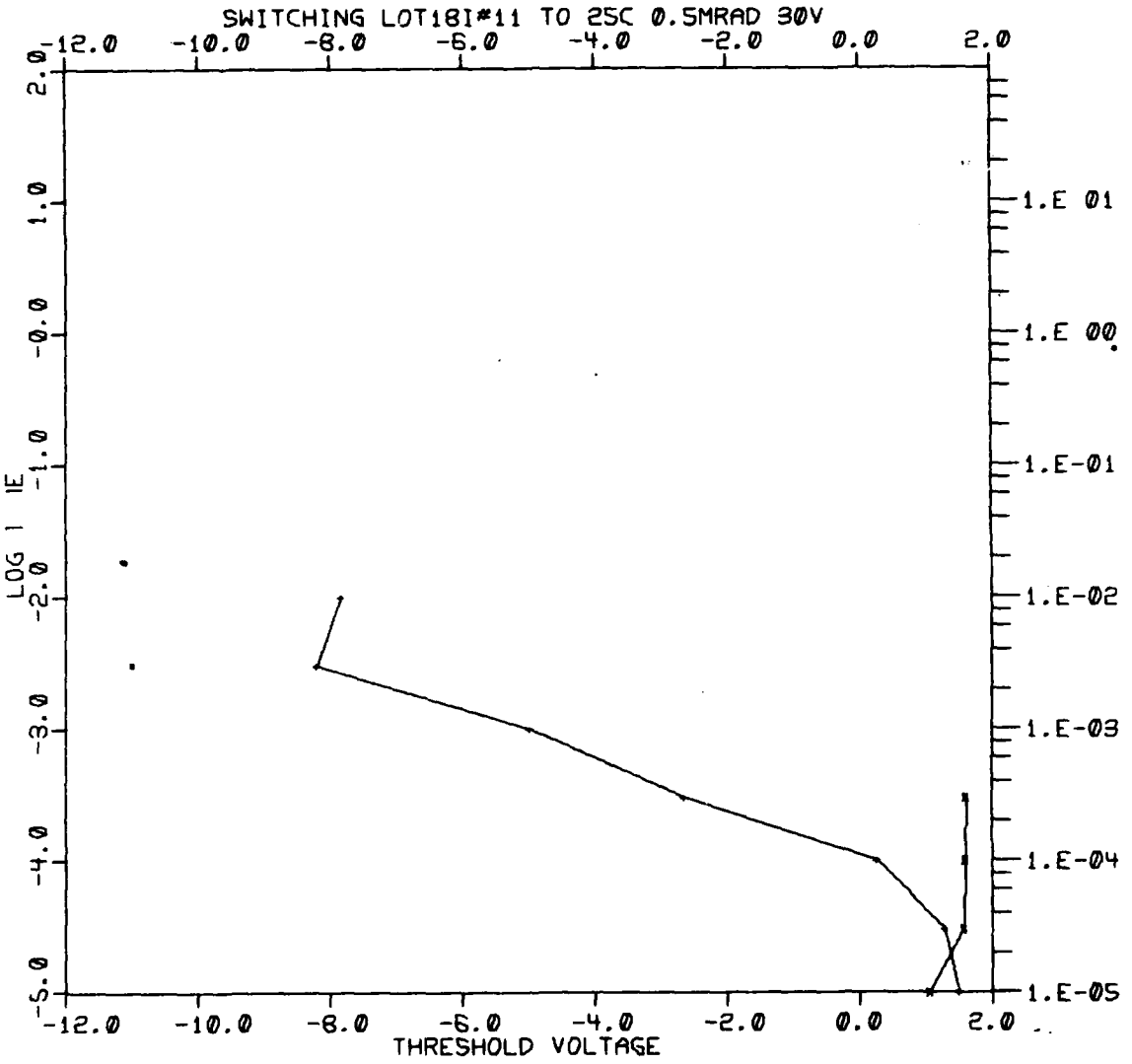

SWITCHING LOT18I#11 TO 25C 0.5MRAD 30V
-12.0
-10.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
2.0
1.0
-0.0
-1.0
-2.0
-3.0
-4.0
-5.0
LOG I IE
1.E 01
1.E 00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
THRESHOLD VOLTAGE

Fig. IV-151

Table IV-5 - Data on Bipolar-Transistor Irradiation Test

Average Values 0.1 Megarad Dose Test

	BETA						At 10V	
	10 μA	100 μA	1 mA	VCEO	VCBO	VEBO	ICEO	VCC(SAT)
Zero Hour	46	64	69	20V	40V	6.9V	<50 nA	135 mV
Irradiated	26	42	52	25V	42V	6.8V	<50 nA	136 mV
Zero Hour	51	60	64	22V	44V	6.9V	<50 nA	145 mV
Irradiated	29	41	54	23V	46V	6.8V	<50 nA	148 mV

Average Values 0.5 Megarad Dose Test

	BETA							
	10 μA	100 μA	1 mA	VCEO	VCBO	VEBO	ICEO	VCC(SAT)
Zero Hour	77	92	94	22V	41.5V	6.9V	<50 nA	144 mV
Irradiated	12.5	30	52	31.5V	44.5V	6.9V	<50 nA	159 mV
Zero Hour	50	65	78	22.5V	37.5V	6.9V	<50 nA	120 mV
Irradiated	17	33	54	24.0V	38.0V	6.9V	<50 nA	130 mV

Table IV-6 - Radiation Test Results of Thin-Oxide and Stepped-Oxide Device at 1×10^5 Rads

Thin Oxide

UNIT NUMBER	PRE RAD V_{TH}	POST RAD V_{TH} LC	POST RAD V_{TH} HC	WINDOW AV
2A - 30	+1.29	-1.76	+1.214	2.9
13A - 75	-3.08	-6.23	+1.3	7.5V
13A - 83	-5.35	-6.93	+1.2	8.1V
18 - 17	-4.6	-4.83	+1.1	5.9

Stepped Oxide

2A - 32	-2.4	-1.07	.519	.5V
13A - 75	-3.1	-7.48	-1.5 V	6 V
13A - 83	-4.3	-7.22	-2.0 V	5 V
18 - 17	-6.4	-8.65	-2.0 V	-6 V

Table IV-7 - Radiation Test Results of Thin-Oxide Device at 5×10^5 Rads

Table IV-7A - Radiation Data - 5×10^5 Rads Thin Oxide MNOS

UNIT	NUMBER	PRE RAD V_{TH}	POST V_{TH} LOW COND	HIGH COND.	WINDOW AV
2A	10	-6.2	-.127	+1.35	1.2 V
	11	-8.1	-2.45	+1.27	3.6 V
	13	-6.2	-.127	+1.3	1.47 V
10A	43	-12	-2.81	+1.31	4.1 V
	45	-10.2	-.86	+1.26	2.06 V
13A	72	-8.2	-4.56	+1.26	5.7 V
	87	-6.7	-3.97	+1.29	5.2 V
18	8	-10.08	+1.51	+1.36	.15 V
	11	-8.75	+1.51	+1.44	.07V

Table IV-7B - Radiation Data - 5 X 10^5 Rads Stepped Oxide

UNIT NUMBER		PRE RAD V_{TH}	POST V_{TH} LOW COND	HIGH COND.	WINDOW AV
2A	10	-10.2	-2.95	-2.34	.6 V
	11	-11.88	-3.71	-2.4	1.3 V
	13	-63	-2.4	-2.39	.1 V
10A	43	-10.2	-3.04	-3.07	.03 V
	45	-9.5	-2.65	-2.69	.04 V
13A	72	-9.9	-4.92	-3.19	1.8 V
	87	-9.9	-4.14	-2.99	1.15 V
18	8	-11.9	-2.2	-2.2	0 V
	11	-10.3	-2.11	-2.11	0 V

Table IV-8 - Radiation Test Results of Thin and Stepped-Oxide Devices at 1 x 10^6 Rads

UNIT NUMBER	PRE RAD V_{TH}	POST RAD V_{TH} LC	POST RAD V_{TH} HC	WINDOW AV
2A - 3		Thin Oxide		
10A 37	+1.2 V	1.25	1.01	.1 V
10A 42	-11.5	1.16	1.11	.05 V
13A 66	-6.25	-3.8	+1.28	5 V
18 7	-8.1	+1.51	+1.45	.06 V
		Stepped Oxide		
2 A 3				
10A 37	+1.4 V	-3.16	-3.26	.01 V
10A 42	-8.4	-2.94	-2.97	.03 V
13A 66	-9.65	-3.74	-2.71	1 V
18 7	-10.8	-2.08	-2.07	.01 V

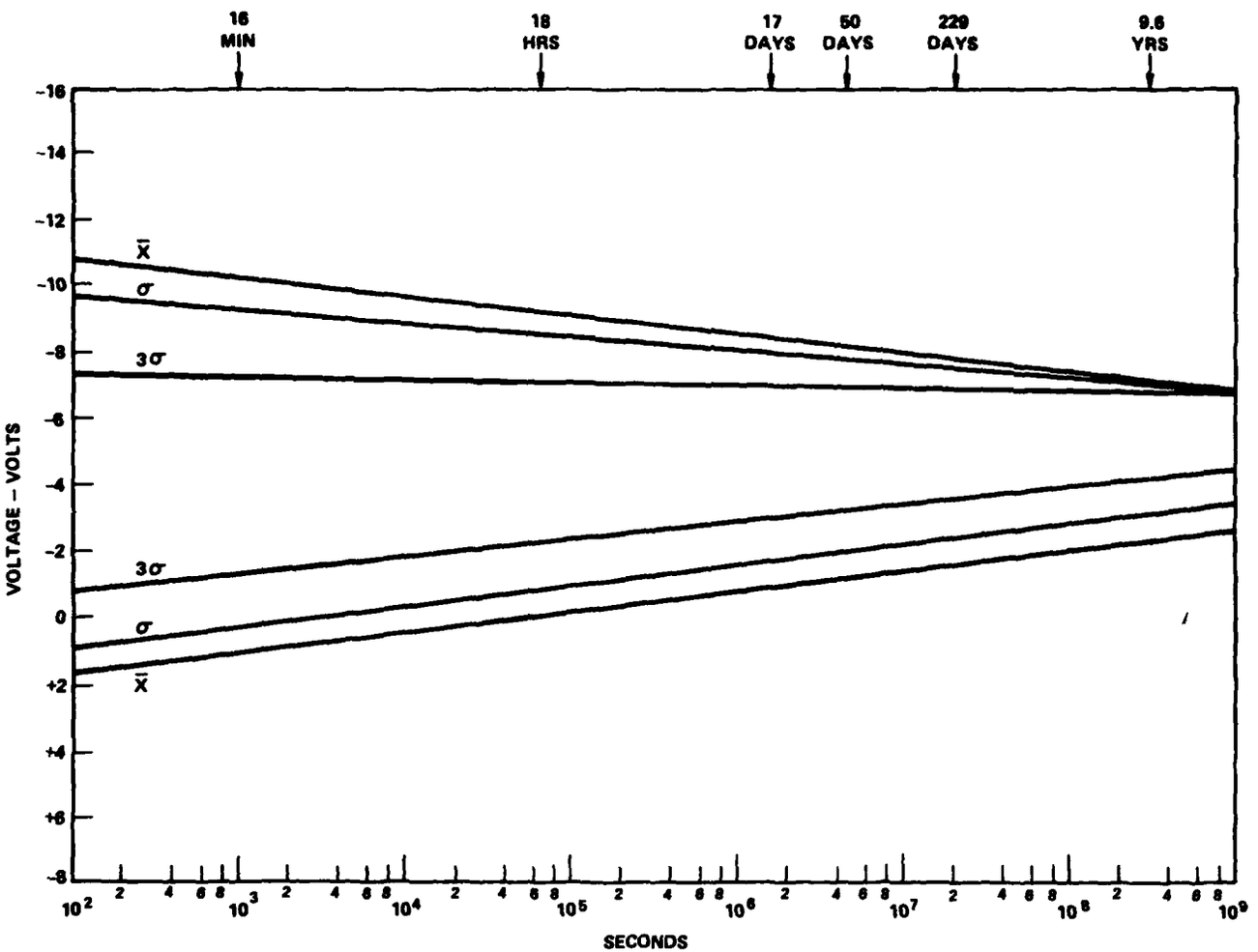


Fig. IV-152 - 25°C storage life.

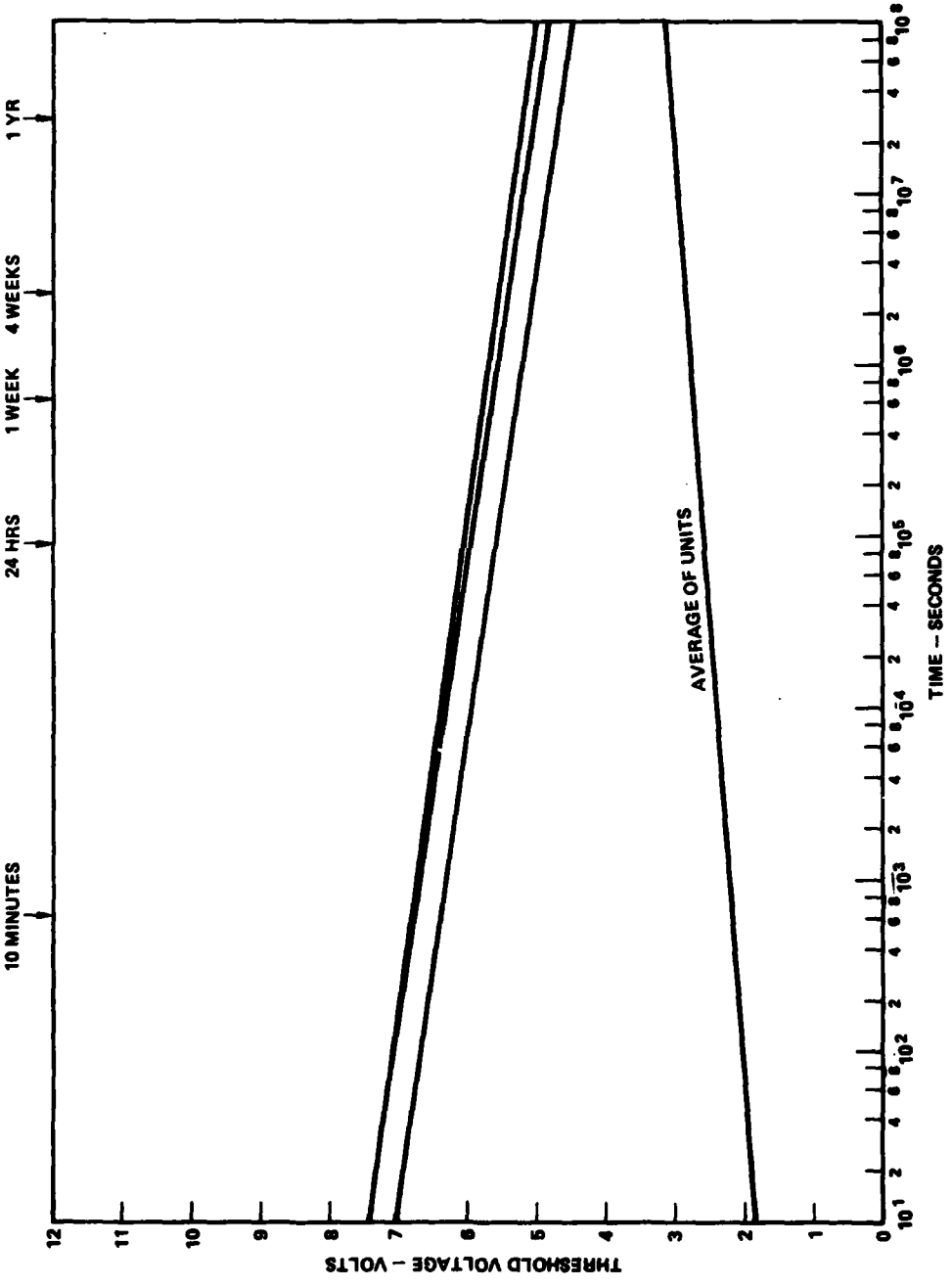
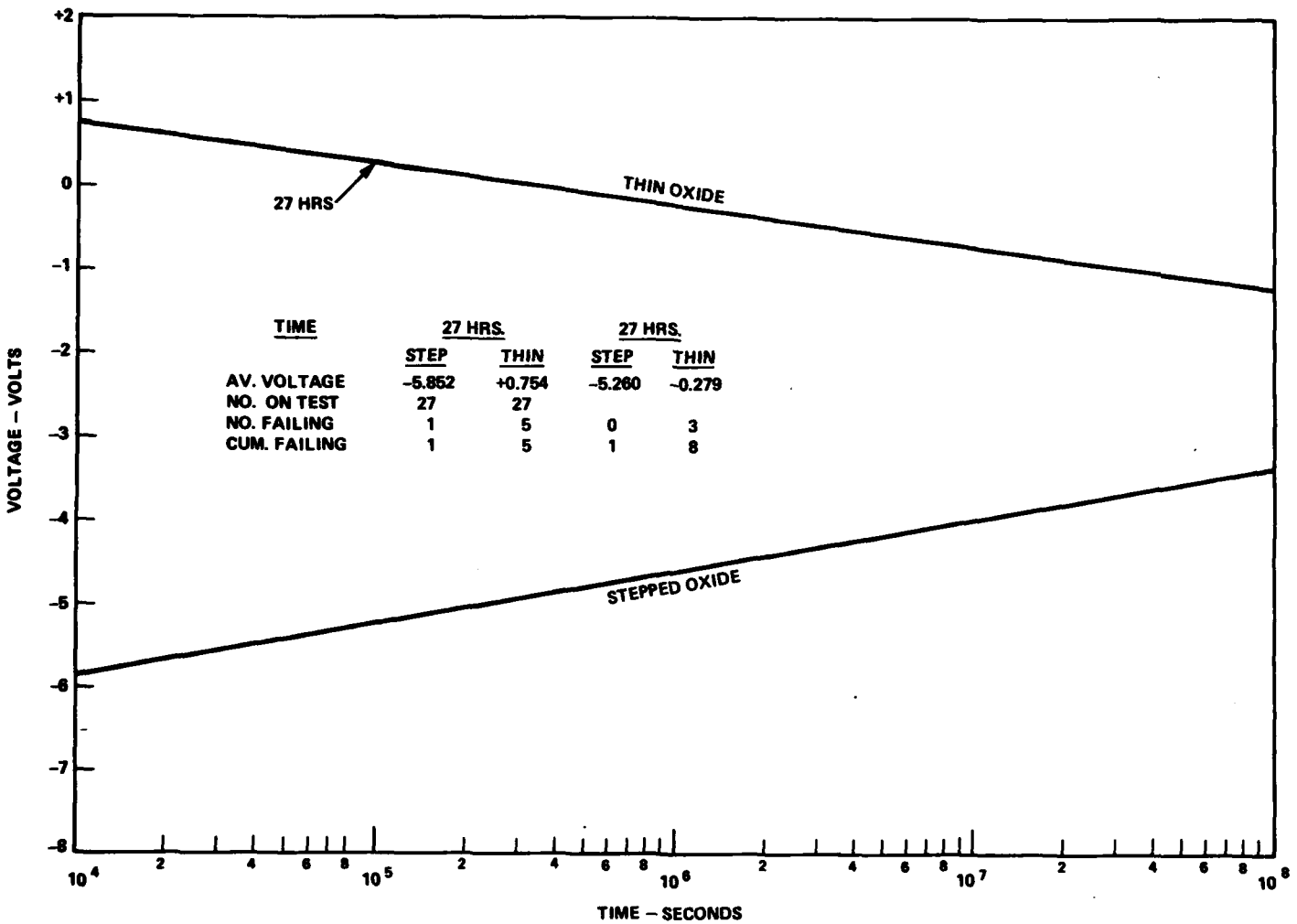


Fig. IV-153 - 150°C storage life.



TIME	27 HRS.		27 HRS.	
	STEP	THIN	STEP	THIN
AV. VOLTAGE	-5.852	+0.754	-5.260	-0.279
NO. ON TEST	27	27		
NO. FAILING	1	5	0	3
CUM. FAILING	1	5	1	8

Fig. IV-154 - Plastic 10^3 programming cycles followed by 100° storage.

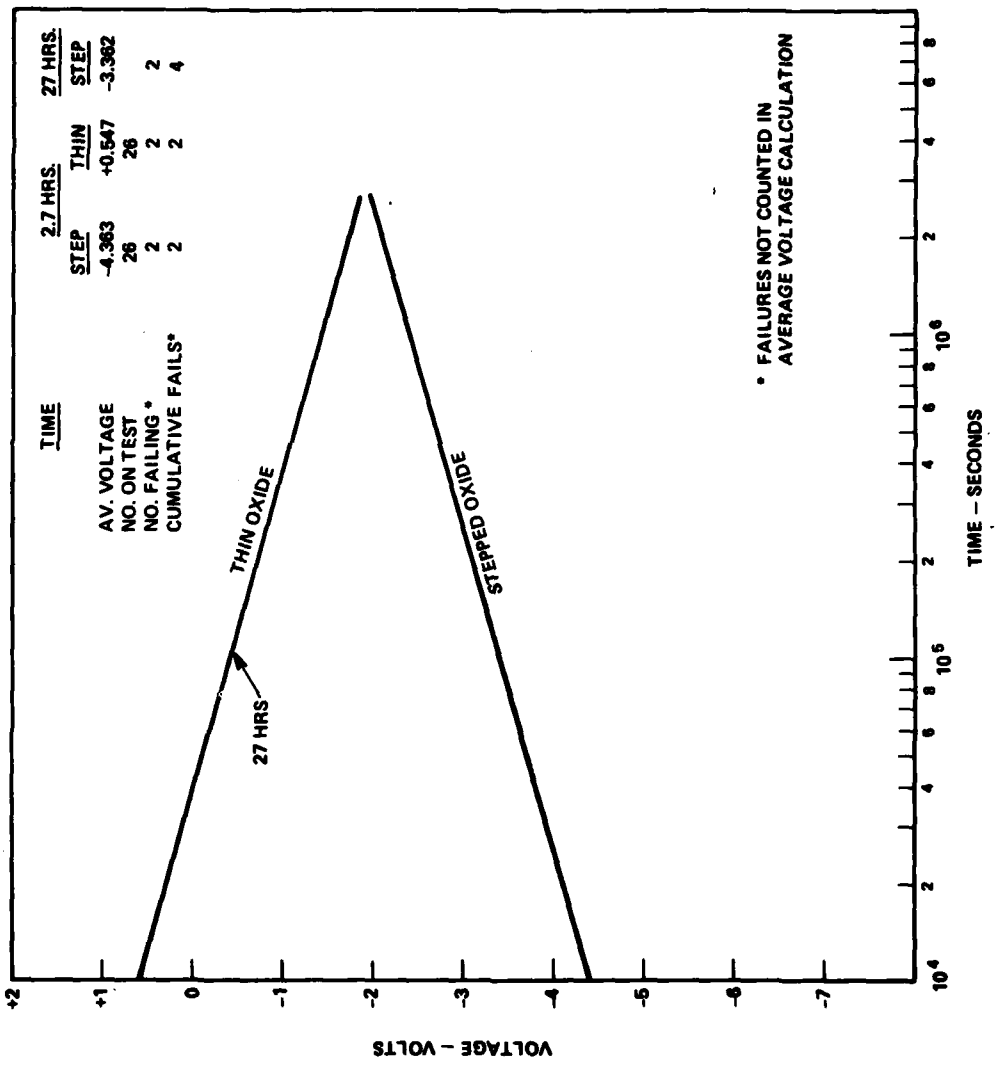


Fig. IV-155 - Ceramic 10^5 programming cycles followed by 100°C storage.

AFSC—Andrews AFB Md 1980

MISSION
of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.